# CHAPTER 12
# Sinusoidal Oscillators

## Learning Objectives

After completing this chapter, you will learn the following:

- Broad classification of oscillators based on the type of output waveform.
- Different constituents of an oscillator circuit.
- Barkhausen criterion of oscillations including gain and phase shift conditions.
- Different types of oscillator circuits.
- RC oscillators including RC phase shift, Wien bridge, Quadrature, Twin-T and Bubba oscillators.
- LC oscillators including Hartley, Colpitt and Clapp oscillators.
- Crystal oscillators including Pierce oscillator.
- Voltage-controlled oscillators.
- Frequency stability considerations.

Discussion on amplifiers is almost invariably followed by the one on oscillators. There are two broad categories of oscillators, namely, the sinusoidal and the non-sinusoidal oscillators. Sinusoidal oscillators discussed in this chapter generate sine wave output. Important types in the non-sinusoidal category are the ones that generate square wave or pulsed outputs. A multivibrator is type of non-sinusoidal oscillator. Multivibrator circuits are discussed in Chapter 13 on wave-shaping circuits. An amplifier is in fact the central building block of an oscillator. While the former has a negative feedback to have increased stability and reduced distortion, the latter is an amplifier with a positive feedback. Major topics discussed in this chapter include oscillator fundamentals like the Barkhausen criterion for oscillations, popular oscillator circuit configurations, which include different types of RC, LC and crystal oscillators and oscillator frequency stability considerations.

## 12.1 Classification of Oscillators

On the basis of the type of output waveform generated, oscillators are classified as *sinusoidal* and *non-sinusoidal* oscillators. Sinusoidal oscillators produce a sine wave output where as non-sinusoidal oscillators produce square or pulsed output. A multivibrator circuit is a type of non-sinusoidal oscillator. Different types of multivibrator circuits are discussed in detail in Chapter 13 on wave-shaping circuits for reasons that would be obvious as we go through the operational basics of the two types of oscillator circuits

in respective chapters. The only thing common between the two types of oscillator circuits is that both types have an inherent regenerative feedback.

Depending upon the nature of the feedback network used, sinusoidal oscillators are further classified as RC, LC and crystal oscillators.

## 12.2 Conditions for Oscillations: Barkhausen Criterion

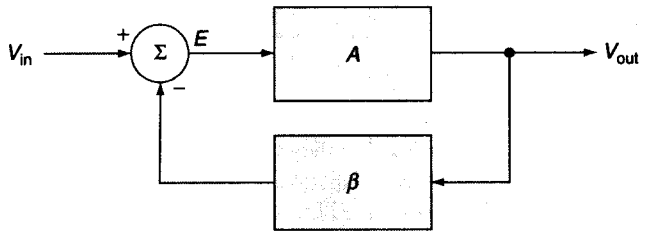
An oscillator circuit is essentially an amplifier circuit with a frequency-selective feedback network. The feedback network feeds a fraction of the amplifier output back to its input in such a way as to satisfy the two fundamental requirements for occurrence of sustained oscillations. These requirements are commonly known by the name of *Barkhausen criterion.*

Barkhausen criterion can be best explained by considering the canonical form of negative and positive feedback systems as shown in Figures 12.1(a) and (b), respectively. Canonical form is the simplest form of representation of any class of systems without any loss of generality. The transfer function in the case of negative feedback system of Figure 12.1(a) can be derived as follows. Remember that in the case of a negative feedback system, the summing point is a subtractor. That is, the error signal is the sum of input signal and the phase-inverted feedback signal:

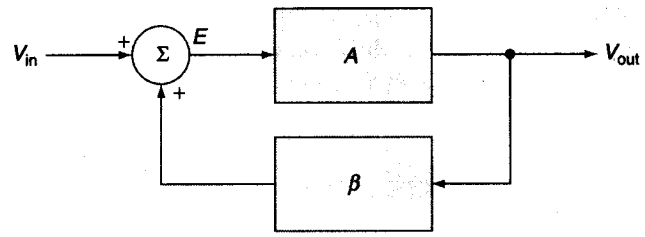
$$E = V_{in} - \beta \times V_{out} \tag{12.1}$$

Substituting $E = V_{out}/A$, we get

$$\frac{V_{out}}{A} = V_{in} - \beta \times V_{out} \tag{12.2}$$




(a)




(b)

**Figure 12.1** Canonical form of feedback systems: (a) Negative feedback system; (b) positive feedback system.

This simplifies to

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+\beta A} \tag{12.3}$$

In the case of a positive feedback system in which the summing point is an adder, the transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{A}{1-\beta A} \tag{12.4}$$

If $\beta A = -1 = 1\angle -180°$ in the case of negative feedback system and $\beta A = 1 = 1\angle 0°$ in the case of positive feedback system, the system works like an oscillator. In the case of the former, the conditions specify magnitude of loop gain as unity and loop phase shift as 180°. In the case of latter, the conditions specify magnitude of loop gain as unity and loop phase shift as 0° or 360°. The condition for the magnitude of the loop gain is the same in the two cases. If we carefully examine the two cases, we will find that the loop phase shift condition in both the cases is also the same as phase inversion implied by the negative sign at the summing point of the negative feedback system restores the overall phase shift at the amplifier input. Essentially the two conditions mean the following:

1. The magnitude of loop gain is unity, which ensures that the feedback signal has the same magnitude as that of the input signal.
2. The magnitude of loop phase shift is such that the feedback signal is in-phase with the input signal when it reaches the input of the amplifier.

These two conditions define what is known as Barkhausen criterion of oscillations. Satisfying Barkhausen criterion ensures that oscillator circuits do not need an external applied input signal. Instead they use fraction of the output signal as the input signal.

In practical oscillator circuits, the summing point is an adder and therefore the Barkhausen criterion of oscillations is written as follows:

1. $|\beta A| = 1$. That is, loop gain should be unity.
2. $\angle \beta A = 0°$ or integral multiple of 360°. That is, loop phase shift should be zero or integral multiple of 360°.

## Initiation of Oscillations

The process of generation of oscillations is initiated due to some inevitable noise present at the amplifier input. The amplified output due to noise has all frequency components. Since the feedback network is a frequency selective one and the loop phase shift condition is satisfied only at one frequency, the signal fed back to the input has a single frequency component at which the loop phase shift condition of the Barkhausen criterion is satisfied. This leads to the oscillator circuit producing a sinusoidal output.

The essential condition for the magnitude of loop gain for oscillations to occur is that loop gain is precisely unity. There is every possibility that with change in parameters of the transistor or other active devices used in the amplifier part of the oscillator due to ageing or replacement, one lands up with loop gain less than unity. In that case there will be no oscillations. So, in practice, loop gain is kept slightly greater than unity to ensure that oscillator works even if there is a slight change in the circuit parameters. Moreover, there is no harm in keeping loop gain slightly greater than unity as the output cannot increase infinitely as it appears because the output amplitude will be limited due to onset of non-linearity of the active device used. However, if magnitude of loop gain is much larger than unity, the oscillator output will have lot of distortion.

## 12.3 Types of Oscillators

Sinusoidal oscillators are classified on the basis of the type of frequency-selective network used in the feedback loop. Different types include the following.

1. RC oscillators;
2. LC oscillators;
3. Crystal oscillators.

### RC Oscillators

In the case of RC oscillators, multiple RC sections are used to provide the required phase shift. Remember that a single section RC or RL network provides up to a maximum of 90° of phase shift due to existence of a single pole in its transfer function. A minimum of two sections would therefore be required to provide the required 180° of phase shift. In practice, cascade arrangement of three RC sections is used in practical RC phase shift oscillators with each section providing 60° of phase shift. This provides a larger value of rate of change of phase with frequency around the operational frequency ($d\phi/d\omega$), which gives improved performance in terms of frequency stability. Frequency stability issues are discussed in detail in the latter part of the chapter. Figure 12.2 shows the plot of phase as a function of frequency in the case of multiple RC sections.

Prominent candidates in the category of RC oscillators include the RC phase shift oscillator, Twin-T oscillator, Wien bridge oscillator, Bubba oscillator and Quadrature oscillator.

### LC Oscillators

A single-section LC circuit has two poles and therefore can provide the required 180° of phase shift. Prominent members include Hartley oscillator, Colpitt oscillator and Clapp oscillator. LC oscillators are suitable for relatively higher operational frequencies due to low-frequency inductors being expensive, bulky and highly non-ideal. RC oscillators are preferred at lower frequencies.

### Crystal Oscillators

In crystal oscillators, crystal resonator provides the electrical equivalent of frequency-selective network. Crystal oscillators are the most stable of the three types due to their extremely high rate of change of phase with frequency at the operating frequency ($d\phi/d\omega$). Crystal oscillators are not practical at lower operating frequencies due to their size, weight and cost restrictions.

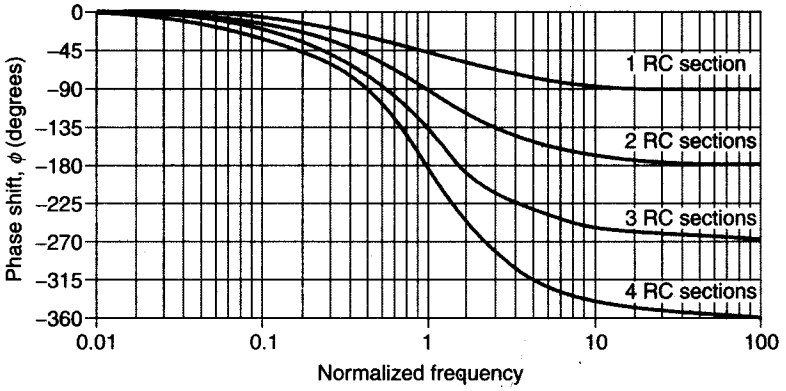



**Figure 12.2** | Phase versus frequency plot of RC sections.

Oscillators belonging to each one of the three above-mentioned categories are described in the following sections.

**EXAMPLE 12.1**

*Determine the gain or phase shift as the case may be for the following oscillator circuits.*

***Case 1:*** *If the feedback network of a certain oscillator provides 1% positive feedback, what should be the minimum gain for the amplifier section of the oscillator for sustained oscillations?*

***Case 2:*** *If in an oscillator, the amplifier portion is a two-stage CE configuration, what should be the phase shift to be introduced by the feedback network at the oscillation frequency for sustained oscillations?*

***Case 3:*** *The amplifier gain in an oscillator is 50. What should be the percentage feedback for sustained oscillations?*

**Solution**

**Case 1**

1. A feedback of 1% means $\beta = 0.01$.
2. Therefore, amplifier's minimum gain is $1/\beta = 100$.

**Case 2**

1. A two-stage CE amplifier provides a phase shift of $2\pi$ radians.
2. Therefore, the feedback network must not introduce any more phase shift or introduce phase shift equal to multiples of $2\pi$ radians in order to satisfy Barkhausen criterion for sustained oscillations.

**Case 3**

1. Amplifier gain = 50.
2. Therefore, feedback factor $\beta = 1/50 = 0.02$.
3. Percentage feedback = 2%.

## 12.4 RC Phase Shift Oscillator

The basic RC phase shift oscillator comprises a single-stage amplifier whose output is fed back to its input through a feedback network. The amplifier portion is usually implemented by either a bipolar junction transistor-based common-emitter amplifier stage or an operational amplifier wired as an inverting amplifier. The feedback network comprises a cascade arrangement of three identical sections of either lag- or lead-type RC network. Figure 12.3 shows the circuit schematic of an RC phase shift oscillator using a common-emitter amplifier stage and a lag-type RC feedback network. This circuit could have been as well implemented using a junction FET-based common-source amplifier stage in place of bipolar junction transistor-based common-emitter stage.

Figure 12.4 shows another version of RC phase shift oscillator in which the amplifier portion is implemented using an operational amplifier configured as an inverting amplifier. In both cases, the amplifier provides a phase shift of 180° at the frequency of operation, which means that the feedback network must also provide an additional phase shift of 180° at the operating frequency to satisfy the loop phase shift condition of the Barkhausen criterion. Also the gain to be provided by the amplifier stage must be at least equal to the inverse of the attenuation factor of the feedback network. In fact, in the phase shift oscillator, while the amplifier gain is dictated by the feedback network attenuation factor; the phase shift provided by the amplifier stage decides the phase shift to be provided by the feedback network.

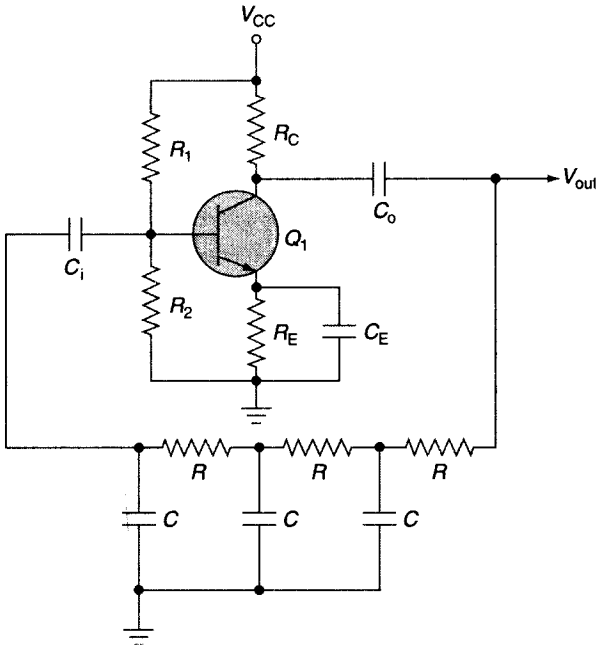



**Figure 12.3** | RC phase shift oscillator with lag-type feedback network using common-emitter amplifier.

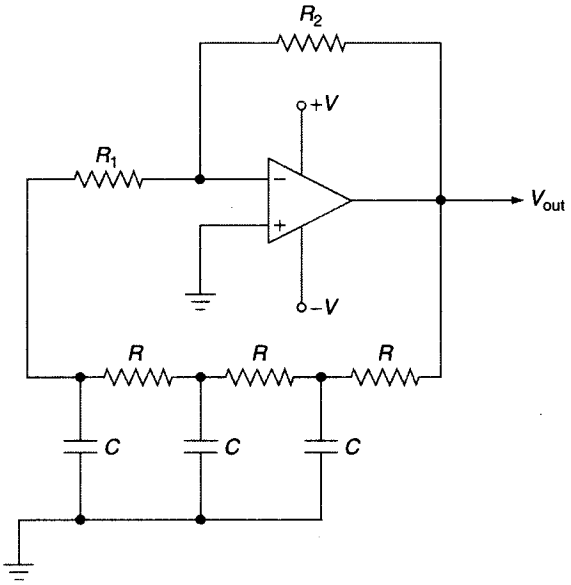



**Figure 12.4** | RC phase shift oscillator with lag-type feedback network using operational amplifier.

In order to analyze the oscillator circuits of Figures 12.3 and 12.4, we need to analyze the transfer function of the feedback network. The transfer function will tell us about both the attenuation and the phase shift provided by this network as a function of frequency.

The transfer function of a single-stage lag-type RC network is give by

$$T(s) = \frac{1}{1 + RCs} \tag{12.5}$$

where $s = j\omega$.

Assuming that the RC sections in the cascade arrangement are independent of each other, that is, individual RC sections do not load each other, then the transfer function of the cascade arrangement of three RC sections is given by

$$T(s) = \left[\frac{1}{1 + RCs}\right]^3 \tag{12.6}$$

Now, the single-section RC network provides a phase shift ($\theta$) given by

$$\theta = \tan^{-1}(-\omega RC) \tag{12.7}$$

$$\tan\theta = -\omega RC$$

$$\omega = -\frac{\tan\theta}{RC} \tag{12.8}$$

If this single RC section were to provide the desired lagging phase shift of 60° so as to produce a total lagging phase shift of 180° from the feedback network, then the operational frequency of the oscillator would be given by

$$\omega = \frac{-\tan(-60°)}{RC} = \frac{\sqrt{3}}{RC}, \text{ which gives } f = \frac{\sqrt{3}}{2\pi RC} \tag{12.9}$$

Attenuation factor provided by single-section RC network is given by

$$\text{Attenuation factor (single-section RC network)} = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}} \tag{12.10}$$

Substituting the value of ($\omega$) from Eq. (12.9), we get

$$\text{Attenuation factor} = 1/\sqrt{(1+3)} = 1/2$$

The overall attenuation factor ($\beta$) of the feedback network is then given by

$$\beta = (1/2)^3 = 1/8 \tag{12.11}$$

Equation (12.11) implies that the amplifier gain must at least be equal to 8. In practice, it is observed that the required gain is much higher than 8 and also that the oscillation frequency is also higher than that computed by using Eq. (12.9). This is due to the loading effect of different RC sections when they are in cascade arrangement. This is explained in the following paragraphs.

Without going into the mathematics of network analysis, considering the loading effect, it can be proved that the transfer function of the three-section RC network of the lag type is given by

$$T(s) = \frac{(1/RC)^3}{s^3 + (5/RC)s^2 + (6/R^2C^2)s + (1/R^3C^3)} \tag{12.12}$$

Substituting $s = j\omega$, we get

$$T(j\omega) = \frac{(1/RC)^3}{[(1/R^3C^3) - (5\omega^2/RC)] + j[(6\omega/R^2C^2) - \omega^3]}$$

Multiplying both numerator and denominator by $R^3C^3$, we get

$$T(j\omega) = \frac{1}{(1-5\omega^2R^2C^2)+j(6\omega RC-\omega^3R^3C^3)} \tag{12.13}$$

If the feedback network were to provide an overall phase shift of 180°, then the imaginary part should be equal to zero. That is, $6\omega RC-\omega^3R^3C^3=0$, which gives

$$\omega = \sqrt{6}/RC \tag{12.14}$$

Substituting the value of $\omega$ in Eq. (12.13), we get the expression for the feedback factor as

$$\text{Feedback factor, } \beta = 1/(1-30) \tag{12.15}$$

This gives

$$|\beta| = 1/29 \tag{12.16}$$

Equations (12.14) and (12.16) specify the required conditions for loop phase shift and loop gain. The oscillation frequency is given by Eq. (12.14) and Eq. (12.16) tells that the amplifier gain must at least be equal to 29.

A similar analysis can be done in the case of lead-type RC phase shift network too. The expressions for the transfer function and the phase shift provided by single-section lead network are given by Eqs. (12.17) and (12.18), respectively.

$$T(s) = \frac{RCs}{1+RCs} \tag{12.17}$$

$$\theta = \tan^{-1}(1/\omega RC)$$

which gives $\omega = 1/\sqrt{3}RC$ for $\theta = 60°$. (12.18)

Considering the loading effect, the transfer function for the cascade arrangement of three-section lead-type RC network is given by Eq. (12.19). This equation is similar to Eq. (12.13) written for the cascade arrangement of lag network.

$$T(j\omega) = \frac{1}{\{1-5/(\omega^2R^2C^2)\}-j\{6/(\omega RC)-1/(R^3C^3\omega^3)\}} \tag{12.19}$$

Again, if the feedback network were to provide an overall phase shift of 180°, then the imaginary part should be equal to zero. That is,

$$6/\omega RC - 1/R^3C^3\omega^3 = 0$$

which gives

$$\omega = 1/(\sqrt{6}RC) \tag{12.20}$$

Substituting the value of $\omega$ in Eq. (12.19), we get expression for the feedback factor:

$$\text{Feedback factor, } \beta = 1/(1-30) \tag{12.21}$$

$$\text{This gives, } |\beta| = 1/29 \tag{12.22}$$

Equations (12.20) and (12.22) specify the required conditions for loop phase shift and loop gain for RC phase shift oscillators employing lead-type RC phase shift network. The oscillation frequency is given by Eq. (12.20) and Eq. (12.22) tells that the amplifier gain must at least be equal to 29. Figure 12.5 shows circuit schematic of RC phase shift oscillator using lead-type phase shift network. The circuit uses opamp-based amplifier stage. The oscillator circuit using transistorized amplifier stage would be similar to the one shown in Figure 12.3 except for the feedback network.

To summarize, in the case of an RC phase shift oscillator, the frequency of oscillation is given by $f = \sqrt{6}/(2\pi RC)$ if the feedback network employed lag-type RC sections and $f = 1/(2\pi\sqrt{6}RC)$ if the feedback circuit used lead-type RC sections. Minimum amplifier gain in both cases is 29.

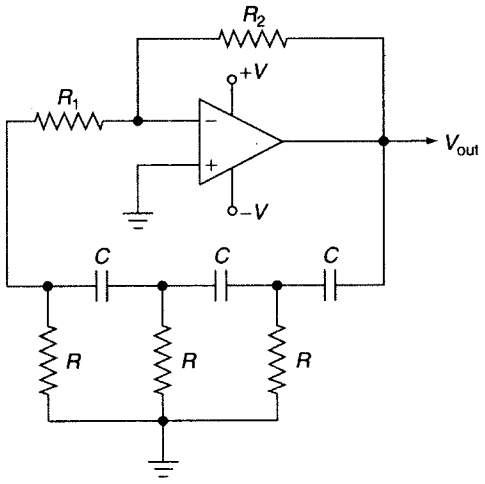



**Figure 12.5** | RC phase shift oscillator with lead-type feedback network using operational amplifier.

RC phase shift oscillator has limitations when it comes to designing a variable frequency oscillator as it is impractical to simultaneously vary three capacitance values equally. Also, adjustment of resistance values is not recommended because variation of resistance values will alter the loop gain of the oscillator circuit and there is likelihood of it not satisfying Barkhausen criterion for sustained oscillations. However, higher $d\phi/d\omega$ resulting from steep phase versus frequency slope provided by the three-section RC network gives a reasonably high frequency stability.

## 12.5 Buffered RC Phase Shift Oscillator

The buffered RC phase shift oscillator (Figure 12.6) overcomes the loading effect of different RC sections in the conventional phase shift oscillator. The oscillator performs very nearly at the computed values of

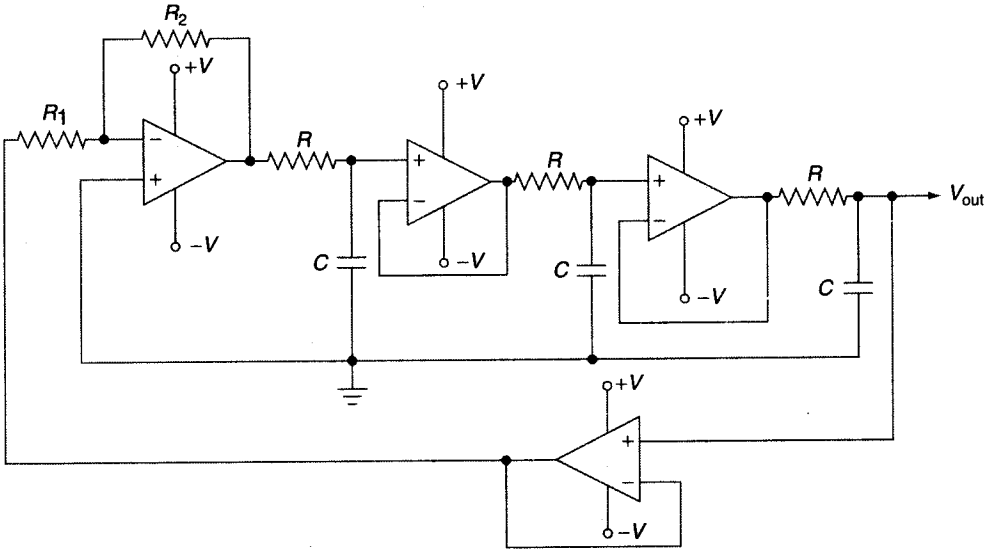



**Figure 12.6** | Buffered RC phase shift oscillator.

frequency and amplifier gain. The oscillation frequency in this case is given by Eq. (12.23) and the minimum value of the amplifier gain for sustained oscillations is 8.

$$f = \sqrt{3}/(2\pi RC) \tag{12.23}$$

In the case of lead-type RC network, the oscillation frequency would be given by

$$f = 1/(2\pi\sqrt{3}RC) \tag{12.24}$$

**EXAMPLE 12.2**

*Refer to the phase shift oscillator of Figure 12.7. Determine the frequency at which this circuit would oscillate if the loop gain criterion were met. Also determine the maximum value of resistance ($R_1$) for sustained oscillations. How would the oscillation frequency change if the positions of R and C in the feedback network were interchanged?*

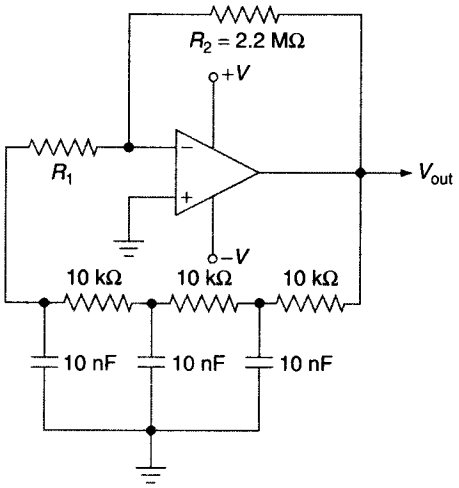



**Figure 12.7** | Example 12.2.

**Solution**

1. The oscillation frequency ($f$) is given by $f = \sqrt{6}/2\pi RC$. Therefore, $f = \sqrt{6}/(6.283 \times 10 \times 10^3 \times 10 \times 10^{-9}) = 3.9$ kHz.
2. Minimum gain to be provided by the amplifier = 29.
3. $|\text{Gain}| = R_2/R_1 = 29$.
4. This gives $R_1 = 2.2 \times 10^6/29 = 75.86$ kΩ.
5. $R_1$ should therefore be less than 75.86 kΩ.
6. When the positions of $R$ and $C$ are interchanged, the oscillation frequency is given by $f = 1/2\pi\sqrt{6}RC$.
7. Substituting the values of $R$ and $C$, we get $f = 650$ Hz.

**EXAMPLE 12.3**

*If in the RC phase shift oscillator circuit of Example 12.2, the three RC sections were separated from each other by opamp buffers. First buffer is connected between the first and second RC sections; second buffer is connected between second and third RC sections and the third buffer is connected between the third RC section and the opamp input. Determine the new values of oscillation frequency and resistor ($R_1$) for sustained oscillations.*

**Solution**

1. The oscillation frequency ($f$) in this case is given by $f=\sqrt{3}/2\pi RC$. Therefore, $f=\sqrt{3}/(6.283 \times 10 \times 10^3 \times 10 \times 10^{-9}) = 2.758$ kHz.
2. Minimum gain to be provided by the amplifier in this case is 8.
3. Therefore, $R_1$ should be less than $2.2 \times 10^6/8 = 275$ kΩ.

**EXAMPLE 12.4**

*Figure 12.8 shows an RC phase shift oscillator using an opamp as the active device. The oscillator is oscillating at the correct frequency but the output is distorted severely near the signal peaks. What could be the possible causes?*

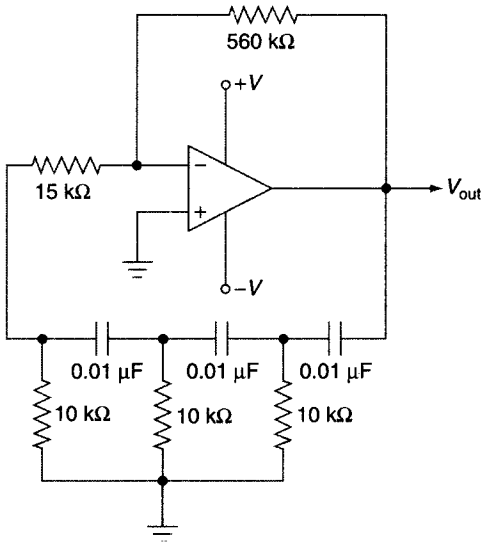



**Figure 12.8** | Example 12.4.

**Solution**

1. The minimum amplifier gain requirement is 29.
2. In order to ensure that we get sustained oscillations and the device replacement and ageing have no effects, the amplifier gain is chosen to be slightly more than what is demanded by the Barkhausen criterion.
3. It may exceed the minimum required gain value by 10–15%. Too large a gain can cause signal clipping near the peaks.
4. The gain magnitude in the present case is given by $560 \times 10^3/15 \times 10^3 \cong 37.3$, which exceeds the required minimum by approximately 30%. This explains the distortion observed in the output.

## 12.6 Bubba Oscillator

Bubba oscillator is a slight variation of the buffered RC phase shift oscillator discussed in Section 12.5. Figure 12.9 shows the circuit schematic of the Bubba oscillator. The difference between the two is that the Bubba oscillator uses four RC sections in the feedback network with each RC section contributing a

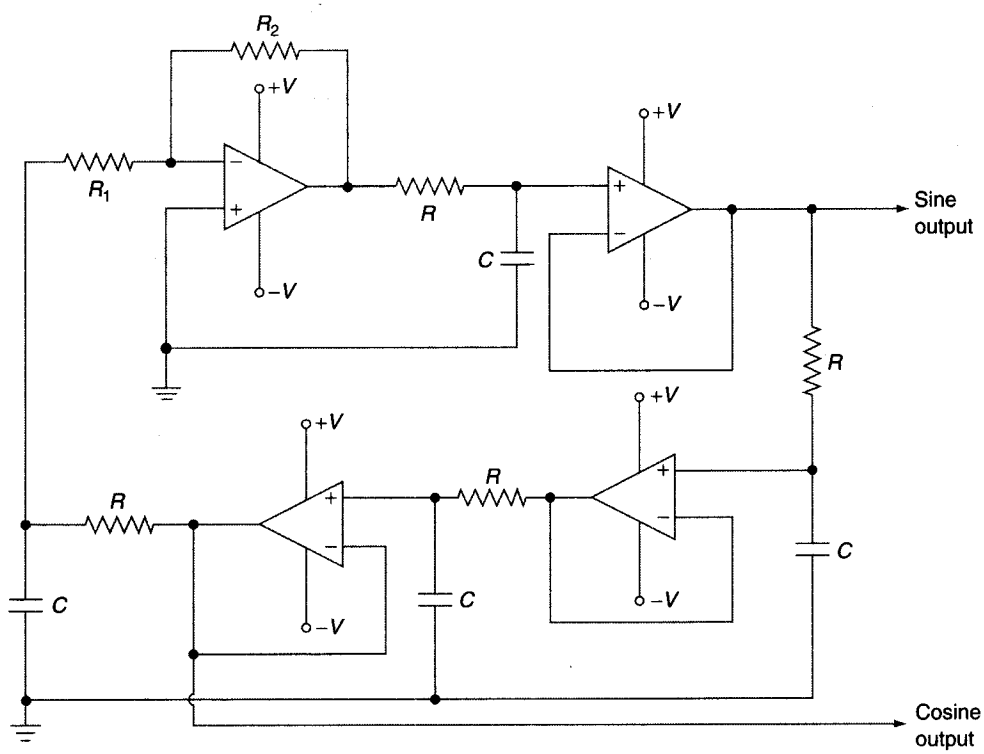



**Figure 12.9** | Bubba oscillator.

phase difference of 45°. This offers two distinctive advantages. One, taking outputs from alternate sections yields low impedance quadrature outputs. Two, use of four RC sections provides higher $d\phi/d\omega$, which in turn leads to relatively higher frequency stability. The expression for the transfer function of the feedback network is given by Eq. (12.25). Remember that different sections in the feedback network are buffered and therefore there is no loading effect.

$$T(s) = \left[\frac{1}{1+RCs}\right]^4 \tag{12.25}$$

Single RC section provides a phase shift of 45° for $\omega = 1/RC$. Substituting for $\omega$ in Eq. (12.25) we get

$$|\beta| = \left|\frac{1}{(1+j)^4}\right| = \frac{1}{4} \tag{12.26}$$

Equation (12.26) tells that the gain of the amplifier must at least be 4 for oscillations to occur. As explained earlier, the gain is chosen to be 10–15% higher than this value.

## 12.7 Quadrature Oscillator

Quadrature oscillator is yet another type of RC phase shift oscillator (Figure 12.10). As is evident from the circuit schematic of Figure 12.10, the circuit employs three RC sections. The circuit takes advantage

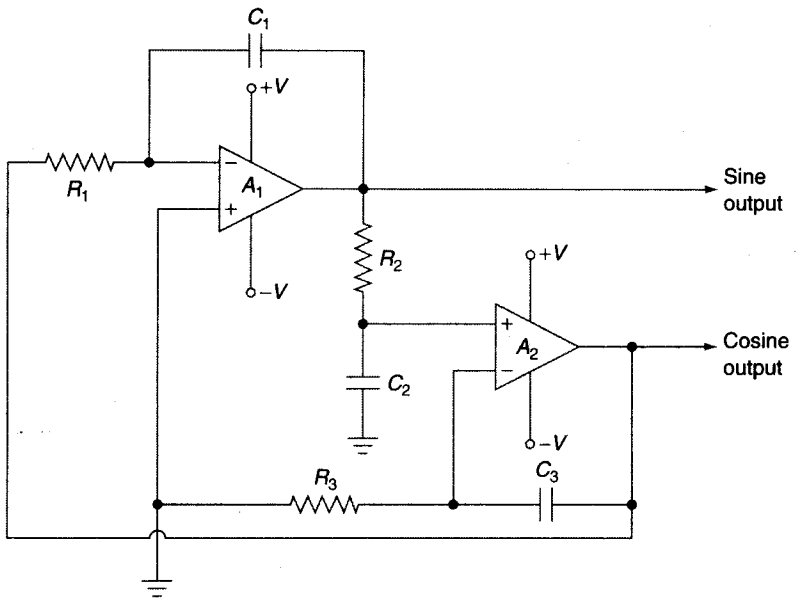



**Figure 12.10** | Quadrature oscillator.

of the fact that double integral of a sine wave is a negative sine wave of the same frequency and phase. This implies that the original waveform is 180° phase-shifted after double integration. The phase of the output from second integrator is then inverted to provide positive feedback to induce oscillations.

The transfer function of the feedback network is nothing but a cascade arrangement of a three networks. The first one comprises $R_1$–$C_1$ configured around opamp $A_1$. The second one comprises $R_2$–$C_2$ and the third one comprises $R_3$–$C_3$ configured around opamp $A_2$. The expression for loop gain is given by

$$\text{Loop gain} = \left[\frac{1}{R_1C_1s}\right] \times \left[\frac{1}{1+R_2C_2s}\right] \times \left[\frac{1+R_3C_3s}{R_3C_3s}\right] \tag{12.27}$$

If $R_1C_1 = R_2C_2 = R_3C_3 = RC$ and if we substitute $\omega = 1/RC$, the first network provides a phase shift of 90°, the second and third networks provide phase shift of 45° so as to provide a total phase shift of 180°. Opamp $A_1$ too provides a phase shift of 180°, which leads to loop phase shift of 0°. Also, Eq. (12.27) reduces to the following equation:

$$\text{Loop gain} = \frac{1}{(RCs)^2} = 1\angle -180° \tag{12.28}$$

The circuit provides sine and cosine outputs (quadrature outputs) because of 90° phase difference between the two signals present at the outputs of the two opamps.

## 12.8 Twin-T Oscillator

The Twin-T oscillator employs a twin-T-type of notch filter network as the frequency selective component in the feedback network. Figure 12.11 shows the basic circuit schematic of a Twin-T oscillator. The circuit employs both positive as well as negative feedback. The positive feedback necessary to produce oscillations is provided by a voltage divider network of $R_1$ and $R_2$. The negative feedback is through the frequency selective twin-T network.

The operational principle of Twin-T oscillator can be best understood by analyzing its transfer function and thereby studying its magnitude and phase response as a function of frequency. In fact, twin-T network is a parallel connection of a lag-type T-network (lower T-network in Figure 12.11) and a lead-type T-network (upper T-network in Figure 12.11). The lag-type T-network causes the magnitude of transfer function to fall and the lagging phase shift angle to increase with increase in frequency. On the other hand, the lead-type T-network causes the magnitude of transfer function to increase and the leading phase shift angle to decrease with increase in frequency. At $\omega = 1/RC$, the two T-networks counter-balance each other with the result that both the magnitude as well as the phase of the transfer function tend to become zero. In fact, at $\omega = 1/RC$, decreasing amplitude response of the lag network counter-balances the increasing amplitude response of the lead network. Also, while lagging phase angle tends to become −90°, the leading phase angle tends to become +90°. Figure 12.12 shows the amplitude and phase response of the twin-T network as a function of normalized frequency. $\omega_c$ equals $1/RC$.

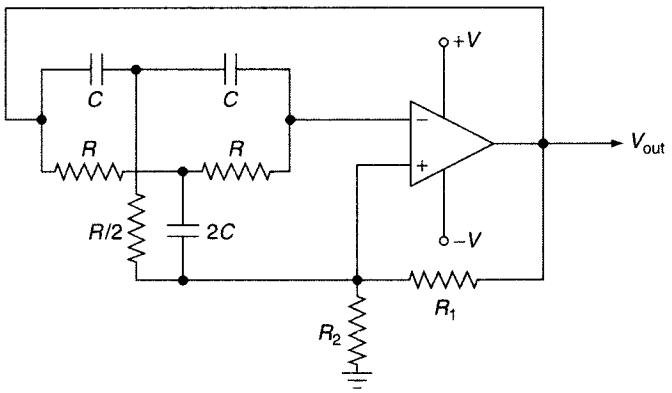



**Figure 12.11** | Twin-T oscillator.

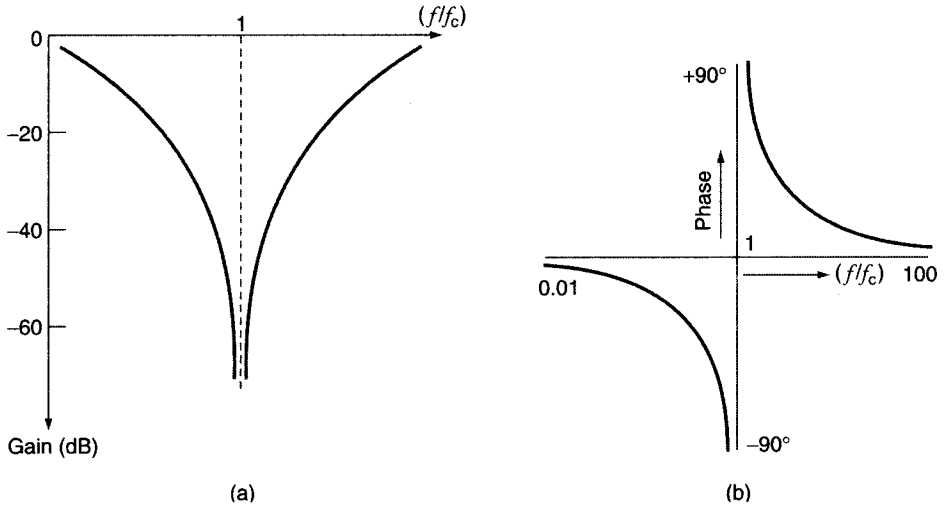



**Figure 12.12** | (a) Magnitude; (b) phase response of twin-T network.

The same can be explained with the help of expression for transfer function of the twin-T network. Without going into mathematical details, the transfer function of the twin-T network can be expressed as

$$T(j\omega)=\frac{1-\omega^2R^2C^2}{1-\omega^2R^2C^2+j4\omega CR} \tag{12.29}$$

The magnitude of $T(j\omega)$ is

$$|T(j\omega)|=\frac{1-\omega^2R^2C^2}{\sqrt{(1-\omega^2R^2C^2)^2+(4\omega CR)^2}} \tag{12.30}$$

The phase angle of $T(j\omega)$ is

$$\theta=\tan^{-1}[4\omega CR/(1-\omega^2C^2R^2)] \tag{12.31}$$

Substituting $\omega = 1/RC$ in Eqs. (12.30) and (12.31), we get the magnitude of transfer function as zero and the phase angle as either −90° or +90°. This small computation thus vindicates what was said in the preceding paragraph.

A zero amplitude for the transfer function implies zero negative feedback at $\omega = 1/RC$. The frequency corresponding to $\omega = 1/RC$ is referred to as notch frequency. At all other frequencies, there will be very high negative feedback thus allowing the circuit to oscillate only very close to the notch frequency. Resistance $R_2$ is a thermistor with a positive temperature coefficient. An incandescent lamp may also be used in place of thermistor. The positive temperature coefficient of resistance of tungsten filament used in incandescent lamp is used for the purpose. A low value of $R_2$ initially produces a large amount of positive feedback to initiate oscillations. Once the oscillations build up, the current flowing through $R_2$ heats it and thus raises its temperature. Increase in temperature increases the value of $R_2$ thus reducing the positive feedback to stabilize the magnitude of oscillations.

Twin-T oscillator produces a low distortion sinusoidal output. This is primarily because of two reasons. First, harmonics are subjected to a very high level of negative feedback, thus severely attenuating them. Second, the operating point of the oscillator is very delicately balanced between positive and negative feedback. This necessitates a very small amount of non-linearity to stabilize the amplitude.

## 12.9 Wien Bridge Oscillator

The *Wien bridge oscillator* is the most widely used RC oscillator configuration for low-frequency applications due to simplicity of the circuit, very good frequency stability and its amenability to variable frequency operation. The only major disadvantage is its relatively higher amplitude distortion unless special measures are taken to minimize it. Modified Wien bridge oscillator designs that minimize distortion are also discussed in the subsequent paragraphs in this section. The basic Wien bridge oscillator circuit comprises a single-stage amplifier whose output is fed back to its input through a feedback network. The amplifier portion is usually implemented by an operational amplifier wired as a non-inverting amplifier. The feedback network comprises a cascade arrangement of a series RC and a parallel RC network. Figure 12.13 shows the circuit schematic of the basic Wien bridge oscillator configured around an operational amplifier.

In order to analyze the oscillator circuit of Figure 12.13, we need to analyze the transfer function of the feedback network. The transfer function will tell us about both the attenuation and the phase shift provided by this network as a function of frequency.

The transfer function of the feedback network can be computed as follows:

1. The impedance of series RC network = $[R_1 + (1/C_1 s)]$.
2. Impedance of parallel RC network = $[R_2/(1 + R_2C_2 s)]$.

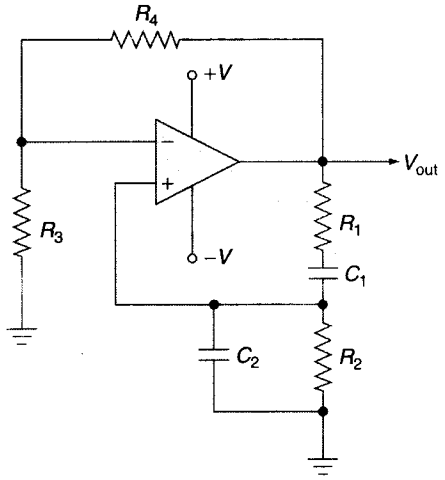



**Figure 12.13** | Basic Wien bridge oscillator.

The transfer function of the feedback network can therefore be written as

$$T(s) = \beta = \frac{R_2 / (1 + R_2 C_2 s)}{(R_1 + 1/C_1 s) + R_2 / (1 + R_2 C_2 s)} \tag{12.32}$$

Equation (12.32) can be simplified to

$$\beta = \frac{R_2 C_1 s}{R_1 C_1 R_2 C_2 s^2 + (R_1 C_1 + R_2 C_2 + R_2 C_1) s + 1} \tag{12.33}$$

Substituting $s = j\omega$ in Eq. (12.33), we get

$$\beta = \frac{j\omega R_2 C_1}{(1 - \omega^2 R_1 C_1 R_2 C_2) + j\omega (R_1 C_1 + R_2 C_2 + R_2 C_1)} \tag{12.34}$$

The magnitude and phase responses of $\beta$ are

$$\text{Magnitude of } \beta, \ |\beta| = \frac{\omega R_2 C_1}{\sqrt{(1 - \omega^2 R_1 C_1 R_2 C_2)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)^2}} \tag{12.35}$$

$$\text{Phase angle, } \theta = 90° - \tan^{-1}[\{\omega (R_1 C_1 + R_2 C_2 + R_2 C_1)\} / (1 - \omega^2 R_1 C_1 R_2 C_2)] \tag{12.36}$$

In order that the loop phase shift is zero, the feedback network must provide a phase shift of zero only. From Eq. (12.36), this implies the following:

$$1 - \omega^2 R_1 C_1 R_2 C_2 = 0$$

which gives the frequency of oscillation as

$$\omega = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \tag{12.37}$$

Substituting for $\omega$ in Eq. (12.35) and simplifying, we get

$$|\beta| = \frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1} \tag{12.38}$$

If in the Wien bridge oscillator, $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then

$$|\beta| = 1/3 \tag{12.39}$$

This implies that the amplifier gain should at least be equal to 3. Also

$$\omega = \frac{1}{RC} \tag{12.40}$$

If we carefully examine the feedback network, we will notice that it is a combination of a lag network formed by $R_1$ and $C_2$ and a lead network formed by $R_2$ and $C_1$. The operating frequency is the geometric mean of the two cut-off frequencies given by $(1/2\pi R_1 C_2)$ and $(1/2\pi R_2 C_1)$.

## Distortion in Wien Bridge Oscillator

As outlined earlier, Wien bridge oscillator is associated with relatively higher output distortion unless design measures are taken to minimize it. High output distortion results from the fact that the output amplitude is at power supply rails. This saturates the output transistors inside the opamp and causes clipping of the output signal at both the supply rails, thus producing several odd and even harmonics.

Distortion can be minimized by applying non-linear feedback. Figure 12.14 shows one such circuit. Initially, diodes $D_1$ and $D_2$ are non-conducting. The feedback resistance in that case is sum of $R_2$ and $R_3$. For larger signals, voltage across $R_3$ is large enough to make $D_1$ and $D_2$ conduct, respectively, during positive and negative half cycles. Conducting diodes ($D_1$ or $D_2$) decrease effective $R_3$, thus reducing the gain.

In another configuration, a non-linear component such as an incandescent lamp or a thermistor with positive temperature coefficient of resistance replaces the gain determining resistance connected from inverting input of the opamp to ground. Figure 12.15 shows the modified circuit schematic. The nominal value of resistance of the non-linear component is chosen to be equal to half of the feedback resistance at the current established by the two resistors. In the absence of any oscillations, the non-linear resistance value will be lower, causing the gain to be

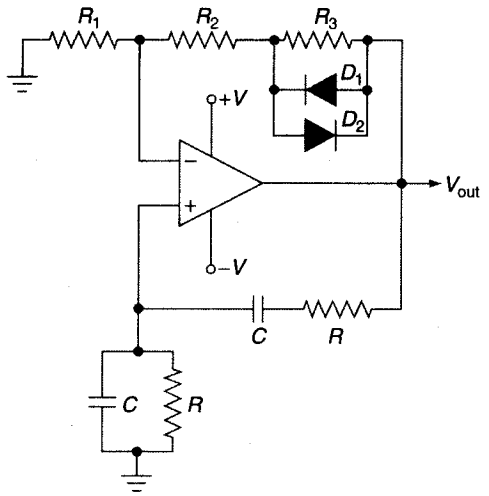



**Figure 12.14** | Wien bridge oscillator with non-linear feedback.

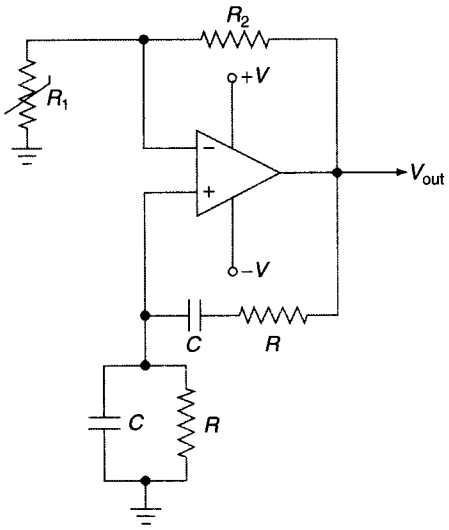



**Figure 12.15** | Wien bridge oscillator with a non-linear resistor.

greater than 3. This initiates oscillations. As the oscillations build up, the current through the non-linear resistance heats it up and causes its resistance to increase thus lowering the gain and stabilizing the output. The non-linear relationship between the current and the resistance ensures that a small change in output voltage causes a large change in the resistance value. This keeps the opamp output away from saturation and hence distortion is minimized. It is observed that the distortion in the circuit of the type shown in Figure 12.15 is more than an order of magnitude better than that observed in the case of oscillator circuit of Figure 12.13.

Another possible circuit configuration that achieves low level of output distortion is shown in Figure 12.16. The circuit employs an N-channel JFET whose drain-to-source ON-resistance $R_{DS(ON)}$ is controlled by a

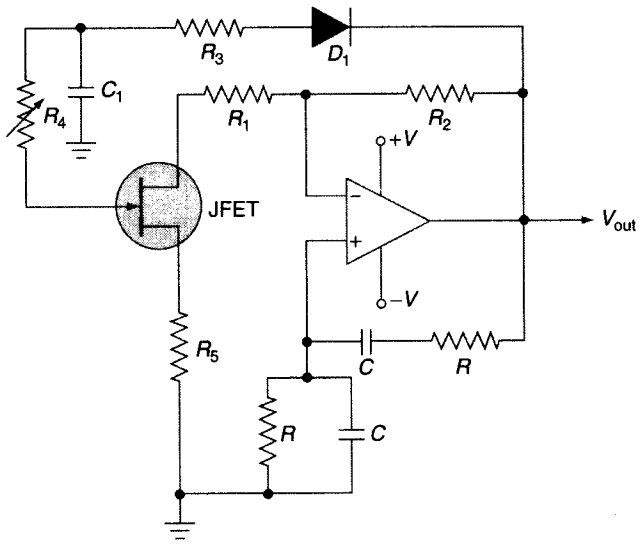



**Figure 12.16** | Wien bridge oscillator with automatic gain control.

negative gate voltage. This negative gate voltage is in turn proportional to the peak amplitude of the output signal. The drain-to-source resistance of the JFET is a part of the gain-determining network as is evident from the circuit. Any increase in output amplitude causes increased negative voltage at the JFET gate terminal. Increased negative voltage causes drain-to-source resistance to increase and therefore the gain to decrease. The circuit arrangement therefore provides automatic gain control. Various resistance values are so chosen as to have an initial gain of greater than 3 to start oscillations. Thereafter, the gain is automatically controlled.

**EXAMPLE 12.5**

*Figure 12.17 shows a buffered RC oscillator circuit. Determine the following:*
*(a) Frequency of oscillation.*
*(b) Possible points in the circuit for quadrature outputs.*
*(c) Value of resistance $R_G$ (choose from 220 kΩ, 290 kΩ, 300 kΩ and 330 kΩ).*

**Solution**

1. The circuit shown is that of Bubba oscillator. It employs four RC sections isolated from each other with opamp buffers.
2. The frequency of oscillation is given by $f = 1/2\pi RC$ as each of the four sections contributes a phase shift of 45°.
3. Therefore $f = 1/(6.283 \times 10 \times 10^3 \times 10 \times 10^{-9}) = 1.592$ kHz.
4. Quadrature outputs may be taken from the outputs of opamps $A_2$ and $A_4$. Remember outputs of $A_2$ and $A_4$ will be 90° apart.
5. Each RC section provides attenuation of $(1/\sqrt{2})$ at the operating frequency.
6. Since RC sections are buffered, attenuation provided by feedback network will be $(1/\sqrt{2})^4 = 1/4$.
7. Therefore the gain of the amplifier should be slightly more than 4.
8. This implies that the input resistance $R_G$ should be slightly less than 300 kΩ. That is, 290 kΩ is the correct choice.

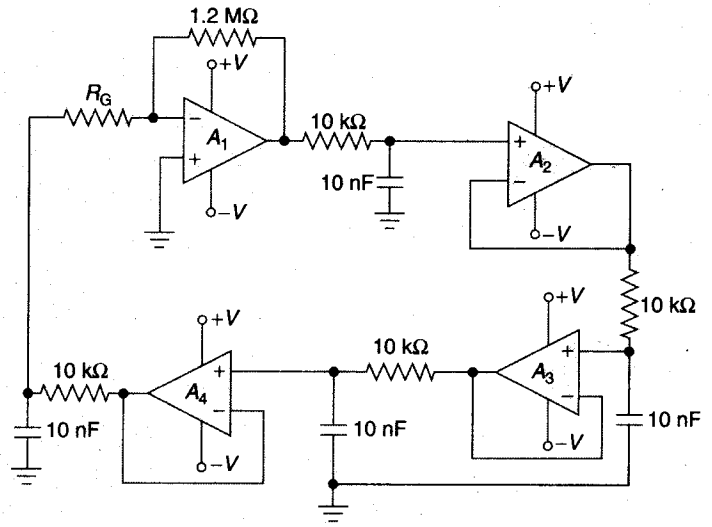



**Figure 12.17** | Example 12.5.

**EXAMPLE 12.6**

*Figure 12.18 shows the circuit diagram of a Quadrature oscillator. Determine the operating frequency. Also determine the phase difference between the signals appearing at the outputs of opamps $A_1$ and $A_2$. If the peak amplitude of the signal appearing at the output of $A_1$ is 2 V, determine the peak amplitude of the signal at the junction of $R_2$ and $C_2$ and also at the output of $A_2$.*

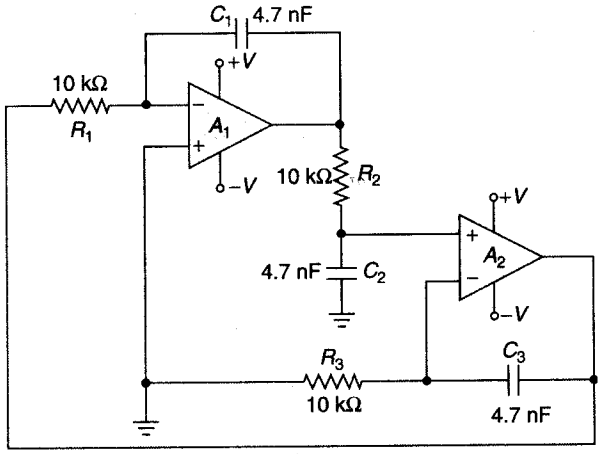



**Figure 12.18** | Example 12.6.

**Solution**

1. The frequency of oscillation is given by $f = 1/2\pi RC$.
2. Substituting the values of $R$ and $C$, we get
$$f = 1/(6.283 \times 10 \times 10^3 \times 4.7 \times 10^{-9}) = 3.386 \text{ kHz}$$
3. The transfer function from output of $A_1$ to junction of $R_2$–$C_2$ is given by $1/(1 + R_2C_2s)$. At $\omega = 1/R_2C_2$, it produces a phase shift of −45°.
4. The transfer function from junction of $R_2$–$C_2$ to the output of $A_2$ is given by $(1 + R_3C_3s)/R_3C_3s$. At $\omega = 1/R_3C_3$, it produces a phase shift of −45°. Since $R_2C_2 = R_3C_3$, the phase shift from output of $A_1$ to the output of $A_2$ will be −90°.
5. It is clear from the transfer functions mentioned above that the two networks respectively provide attenuation and gain of $1/\sqrt{2}$ and $\sqrt{2}$.
6. Therefore, peak amplitude of signal at junction of $R_2$–$C_2$ is $2/\sqrt{2} = \sqrt{2}$ V and that at the output of $A_2$ is $\sqrt{2} \times \sqrt{2} = 2$ V.

**EXAMPLE 12.7**

*Refer to the Twin-T oscillator of Figure 12.19. Determine the frequency of the output signal. How would the frequency change if all component values in the twin-T network are doubled?*

**Solution**

1. The operating frequency ($f$) is given by $f = 1/2\pi RC$.
2. If we compare the given twin-T network with the standard form of twin-T, we will find that $R = 2 \times 10 \times 10^3\ \Omega = 20\ \text{k}\Omega$ and $C = 0.01 \times 10^{-6}/2 = 0.005\ \mu\text{F}$.
3. Therefore, $f = 1/(6.283 \times 20 \times 10^3 \times 0.005 \times 10^{-6}) = 1.592$ kHz.

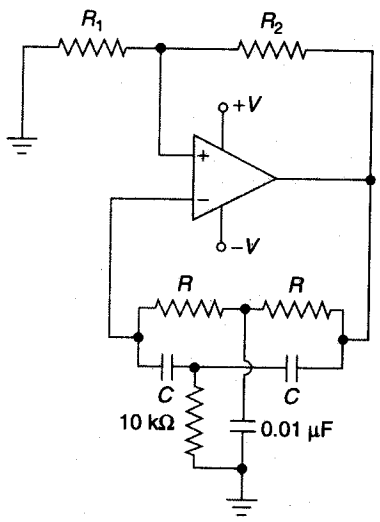



**Figure 12.19** | Example 12.7.

4. When all component values are doubled, the operating frequency will be reduced to one-fourth. That is, changed value of frequency = 1.592/4 = 398 Hz.

**EXAMPLE 12.8**

*Refer to the Wien bridge oscillator circuit of Figure 12.20. Determine the oscillator frequency and the preferred value of* $R_1$.

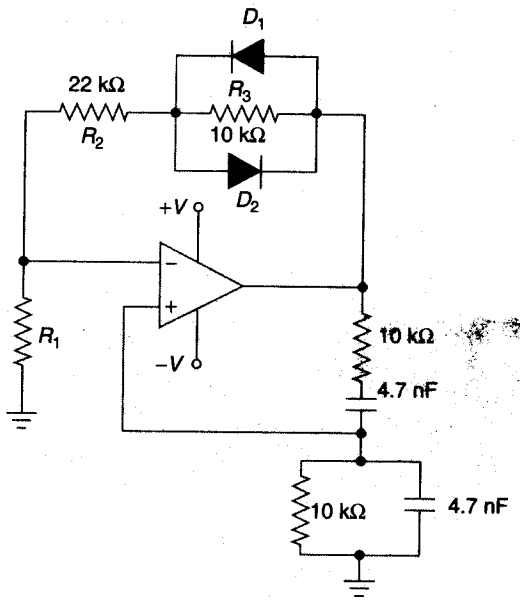



**Figure 12.20** | Example 12.8.

**Solution**

1. Oscillator frequency is given by $f = 1/2\pi RC$ where $R = 10$ kΩ and $C = 4.7$ nF.
2. Therefore, $f = 1/(6.283 \times 10 \times 10^3 \times 4.7 \times 10^{-9}) = 3.386$ kHz.
3. Required minimum value of amplifier gain = 3.
4. Amplifier gain = $1 + [(R_2 + R_3)/R_1]$.
5. This gives $(R_2 + R_3)/R_1 = 2$, $R_1 = (22 \times 10^3 + 10 \times 10^3)/2 = 16 \times 10^3\ \Omega = 16$ kΩ.
6. Since the required gain has to be slightly greater than 3, preferred value of $R_1$ therefore should be slightly less than 16 kΩ.
7. $R_1$ may be chosen to be 15 kΩ.

**EXAMPLE 12.9**

*Refer to the RC oscillator circuit of Figure 12.21. Identify the type of oscillator. Also, determine the operating frequency and preferred value of $R_3$.*

**Solution**

1. It is Wien bridge oscillator.
2. Operating frequency is given by $\omega = 1/\sqrt{R_1R_2C_1C_2}$. Therefore, $\omega = 1/\sqrt{10^3 \times 100 \times 10^3 \times 0.1 \times 10^{-6} \times 10^{-9}} = 10^4$ rad/s.
3. $f = \omega/2\pi = 10^4/6.283$ Hz = 1.592 kHz.
4. Attenuation provided by feedback network is given by
$$|\beta| = R_2C_1/(R_1C_1 + R_2C_2 + R_2C_1)$$
$$|\beta| = (100 \times 10^3 \times 0.1 \times 10^{-6})/(10^3 \times 0.1 \times 10^{-6} + 100 \times 10^3 \times 10^{-9} + 100 \times 10^3 \times 0.1 \times 10^{-6})$$
$$= 10^{-2}/(10^{-4} + 10^{-4} + 10^{-2}) = 1/1.02$$
5. Therefore, minimum value of required gain = 1.02. That is, $1 + (R_4/R_3) = 1.02$, $R_4/R_3 = 0.02$.
6. $R_3 = 2.2 \times 10^3/0.02 = 110$ kΩ.
7. Since the required gain has to be slightly greater than 1.02, preferred value of $R_3$ therefore should be slightly less than 110 kΩ.
8. $R_3$ may be chosen to be 100 kΩ.

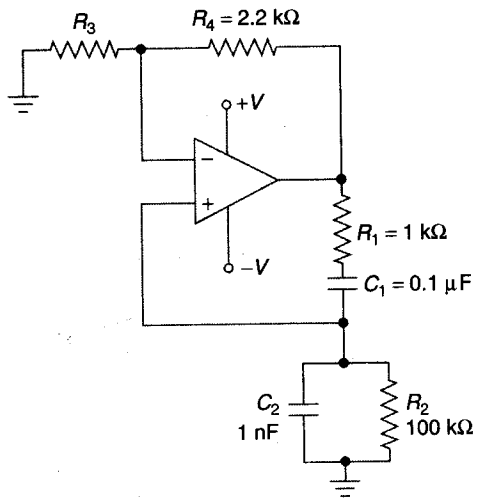



**Figure 12.21** | Example 12.9.

## 12.10 LC Oscillators

As outlined earlier, in essence, every oscillator has three main sections. These are the amplifier, the frequency-determining network and the feedback arrangement. The frequency-determining network decides the operating frequency and the feedback arrangement ensures that part of the output signal fed back to the input has the correct amplitude and phase at the operating frequency. In fact, the feedback network together with the amplifier ensures that Barkhausen criterion for sustained oscillations is satisfied at the operating frequency.

In the case of LC oscillators, the operating frequency is determined by an LC tank circuit and is given by $(1/2\pi\sqrt{LC})$. The exact frequency of oscillation is determined by $(1/2\pi\sqrt{LC}) \times \sqrt{Q^2/(Q^2+1)}$. Here $Q$ is the quality factor of the tank circuit. The amplifier may be configured around a bipolar transistor, a junction FET, a MOSFET or an operational amplifier.

LC oscillators are usually classified by the name of its inventor. The common ones are Armstrong oscillator, Hartley oscillator, Colpitt oscillator and Clapp oscillator. They are also classified as series-fed or shunt-fed oscillators depending upon the manner in which DC power is applied to the active device. In the case of series-fed LC oscillators, DC power is applied to the active device through the tank circuit or a part of the tank circuit. In shunt-fed LC oscillators, DC power is applied through a separate path that is parallel to the tank circuit. Each of the LC oscillators mentioned in the preceding paragraph can be constructed either way.

Also, LC oscillators (Armstrong, Hartley, Colpitt and Clapp) are identifiable by the manner in which feedback signal is coupled to the input. In the case of Armstrong oscillator, the feedback signal is magnetically coupled [Figure 12.22(a)]. In the case of Hartley oscillator, a tapped or a split coil is used for the purpose [Figure 12.22(b)]. Split capacitor arrangement is used in the case of Colpitt and Clapp oscillators [Figure 12.22(c)]. Each of these oscillators is described in the following sections.

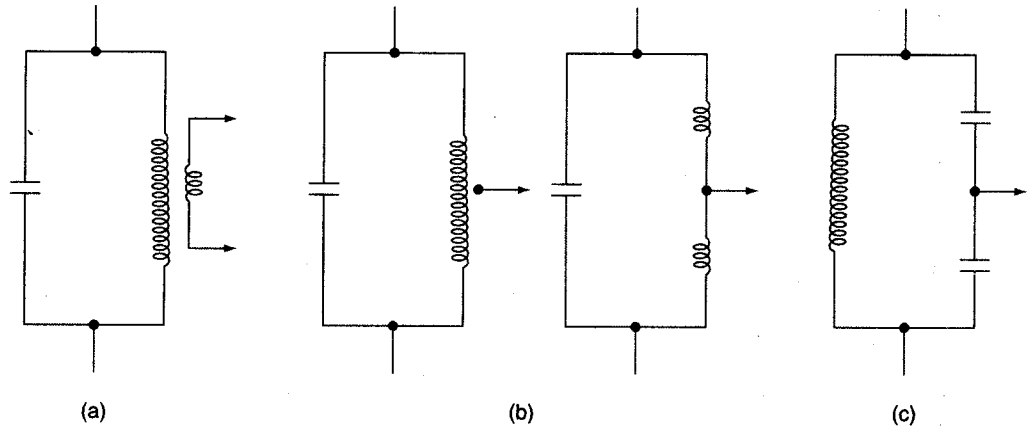



**Figure 12.22** | Feedback coupling arrangement in LC oscillators.

## 12.11 Armstrong Oscillator

Armstrong oscillator, also known as Meissner oscillator, uses magnetic coupling as means of feeding part of output signal back to input to provide oscillations. It is also called a Tickler oscillator due to use of magnetic coupling between the tickler coil and the coupling coil. Tickler coil is the name given to a small coil connected in series with the plate circuit of a vacuum tube and coupled inductively to the grid circuit to provide feedback. In the case of a BJT or an FET, the tickler coil is placed in series with the collector or drain circuit and is inductively coupled to the base or gate circuit. A capacitor is placed across either the coupling coil or the tickler coil to form a tank circuit that decides the operating frequency.

Figures 12.23(a) and (b) show the basic circuit arrangements in the two cases with n-channel junction FET used as the active device. Biasing components are omitted for the sake of simplicity.

The frequency of oscillation is primarily determined by the tank circuit and is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{12.41}$$

Here $L$ is the inductance of the coupling coil in the case of circuit shown in Figure 12.23(a) and that of tickler coil in the case of circuit shown in Figure 12.23(b). In practice, the frequency of oscillations is slightly different from the one computed by using Eq. (12.41) because of stray capacitances, loading of tank circuit, etc. The feedback factor in this case is given by ratio of mutual inductance between the two coils to the inductance in the tank circuit. Minimum gain required to start oscillations is reciprocal of the feedback factor.

Figure 12.24 shows the circuit schematic of an Armstrong oscillator configured around a bipolar junction transistor. The transistor is wired in common-emitter configuration and thus provides a phase shift of

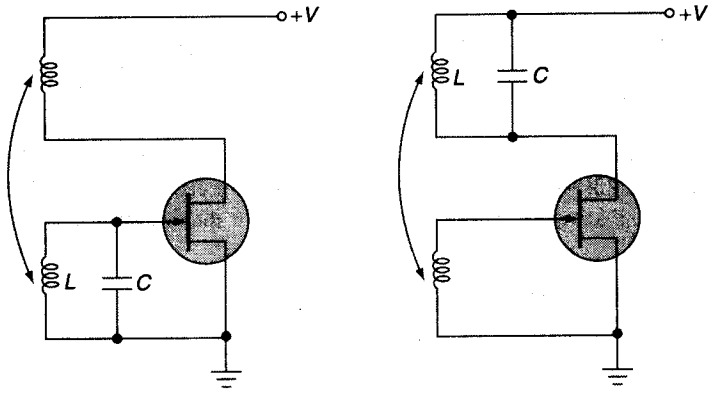



**Figure 12.23** | Basic Armstrong oscillator configurations.

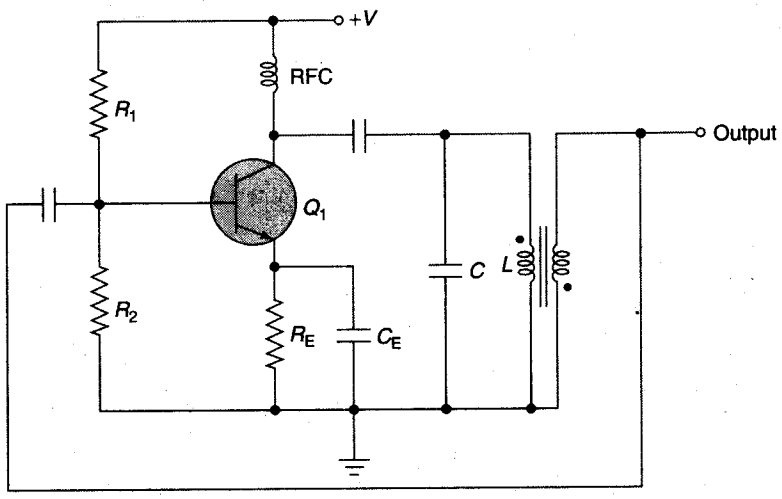



**Figure 12.24** | Shunt-fed Armstrong oscillator.

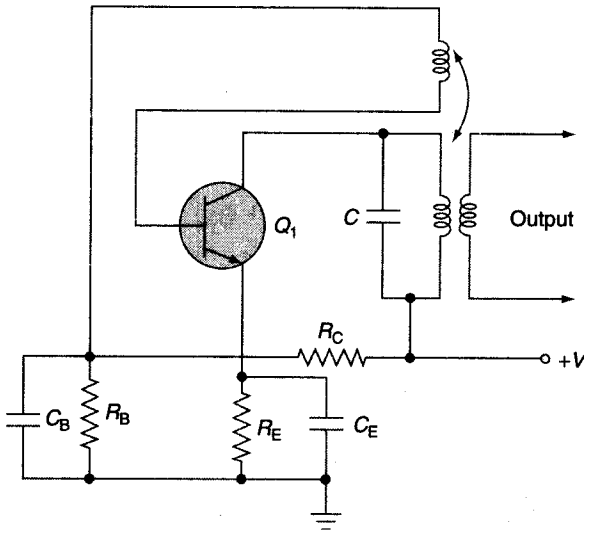



**Figure 12.25** | Series-fed Armstrong oscillator.

180°. Another 180° phase shift is provided by magnetic coupling as indicated by placement of dots. Operating frequency is decided by tank circuit comprising capacitor $C$ and inductance $L$ of transformer primary. Note that Armstrong oscillator of Figure 12.24 is a shunt-fed oscillator. The circuit schematic of a series-fed Armstrong oscillator would look like the one shown in Figure 12.25.

## 12.12 Hartley Oscillator

Hartley oscillator uses a tapped or split coil for the purpose of generating feedback signal. This is where a Hartley oscillator differs from an Armstrong oscillator, which uses a separate coil called tickler coil. In the case of Hartley oscillator, current flowing through one section of the tapped coil induces a voltage in the other section to provide feedback. The feedback signal is 180° out-of-phase with the one that produces it.

Figure 12.26 shows the circuit schematic of Hartley oscillator configured around a bipolar junction transistor. Incidentally, the circuit shown is that of a series-fed oscillator. Figure 12.27 shows the Hartley oscillator configured around an opamp.

The attenuation factor and the phase shift provided by the feedback network can be determined from the transfer function of the feedback network. The feedback network in the present case is a π-network with capacitive series element and inductive shunt elements. The transfer function is given by

$$T(j\omega) = \beta = \frac{-\omega^2 L_2 C}{1-\omega^2 L_2 C} = \frac{-(1-\omega^2 L_1 C)}{\omega^2 L_1 C} \tag{12.42}$$

Negative sign implies phase shift of 180°. Also,

$$|\beta|^2 = \left[\frac{\omega^2 L_2 C}{1-\omega^2 L_2 C}\right] \times \left[\frac{1-\omega^2 L_1 C}{\omega^2 L_1 C}\right]$$

$$= \left(\frac{L_2}{L_1}\right) \times \left[\frac{1-\omega^2 L_1 C}{1-\omega^2 L_2 C}\right]$$

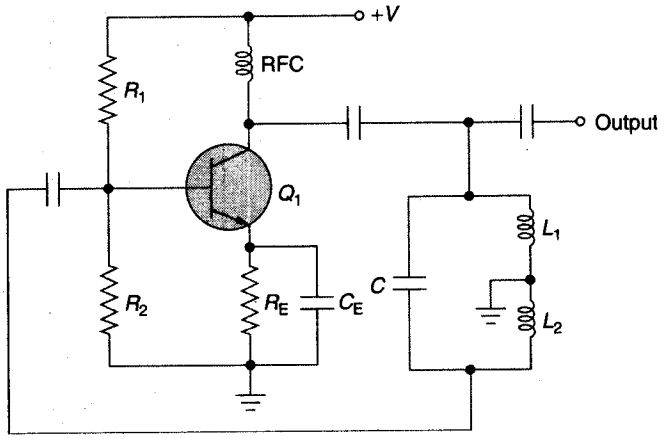



**Figure 12.26** | Hartley oscillator configured around bipolar junction transistor.

Substituting $\omega = 1/\sqrt{(L_1 + L_2)C}$, we get

$$|\beta|^2 = \left(\frac{L_2}{L_1}\right)^2 \tag{12.43}$$

$$|\beta| = \left(\frac{L_2}{L_1}\right)$$

Equations (12.42) and (12.43) imply that the feedback network introduces a phase shift of 180° and signal attenuation by a factor of $(L_2/L_1)$ at the operating frequency $(\omega)$ provided that $\omega = 1/\sqrt{(L_1 + L_2)C}$. This further implies that the amplifier must provide a gain of greater than $L_1/L_2$ to satisfy the loop gain criterion and a phase shift of 180° to satisfy the loop phase shift criterion.

The advantage of using Hartley oscillator lies in its capability to generate a wide range of frequencies and its easy tunability.

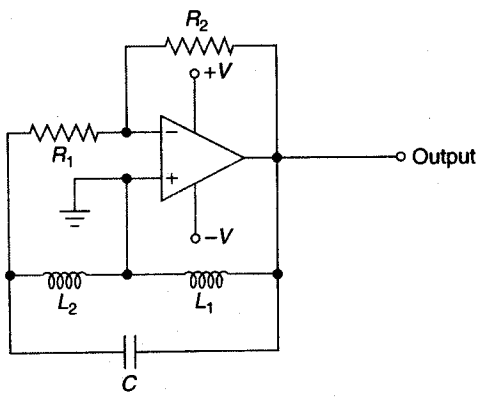



**Figure 12.27** | Hartley oscillator configured around opamp.

## 12.13 Colpitt Oscillator

Colpitt oscillator uses a pair of capacitors and an inductor in the tank circuit to produce the regenerative-feedback signal. In fact, the feedback network in this case is an electrical dual of the feedback network of Hartley oscillator. Figures 12.28 and 12.29 show the Colpitt oscillator circuits configured around bipolar junction transistor and opamp, respectively. An FET could also be used as the active device instead. As is obvious from the two circuit schematics, the output signal is developed across $C_1$ and the feedback signal is generated across $C_2$.

The attenuation factor and the phase shift provided by the feedback network can be determined from the transfer function of the feedback network. The feedback network in the present case is a $\pi$-network with inductive series element and capacitive shunt elements. The transfer function is given by

$$T(j\omega) = \beta = -(\omega^2 LC_1 - 1) = \frac{-1}{\omega^2 LC_2 - 1} \tag{12.44}$$

Negative sign implies phase shift of 180°. We will subsequently see that for $\omega = 1/\sqrt{LC_1C_2 / (C_1 + C_2)}$, both $(\omega^2 LC_1 - 1)$ and $(\omega^2 LC_2 - 1)$ are positive.

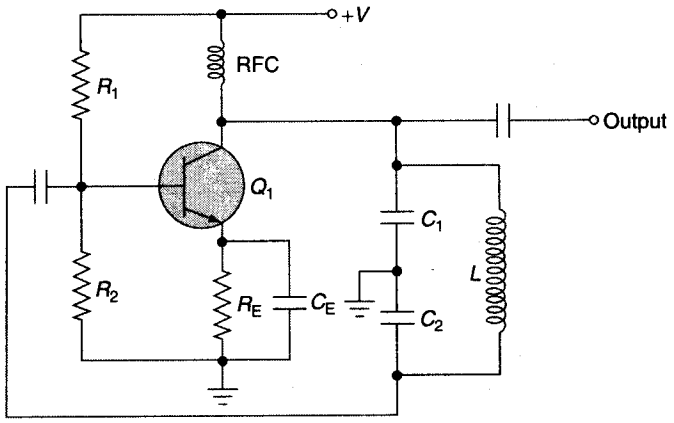



**Figure 12.28** | Colpitt oscillator configured around bipolar transistor.

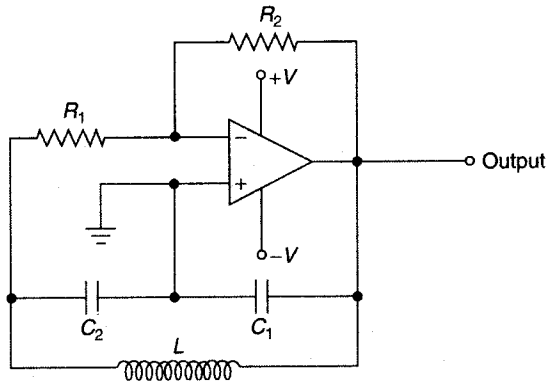



**Figure 12.29** | Colpitt oscillator configured around opamp.

Also,

$$|\beta|^2 = \frac{\omega^2 LC_1 - 1}{\omega^2 LC_2 - 1}$$

For $\omega = 1/\sqrt{LC_1C_2/(C_1 + C_2)}$, this simplifies to

$$|\beta| = \frac{C_1}{C_2} \tag{12.45}$$

Equations (12.44) and (12.45) imply that the feedback network introduces a phase shift of 180° and signal attenuation by a factor of $C_1/C_2$ at the operating frequency ($\omega$) provided that $\omega = 1/\sqrt{LC_1C_2/(C_1 + C_2)}$. This further implies that the amplifier must provide a gain of greater than $(C_2/C_1)$ to satisfy the loop gain criterion and a phase shift of 180° to satisfy the loop phase shift criterion.

In practice, the operating frequency is affected by the junction capacitance whose Miller components appear across $C_1$ and $C_2$. This is overcome in Clapp oscillator configuration.

## 12.14 Clapp Oscillator

Clapp oscillator circuit is a slight modification of the Colpitt oscillator circuit configuration. The feedback circuit in the case of Clapp oscillator uses an extra capacitor ($C_3$ in Figure 12.30) in series with the coil. The function of $C_3$ is to minimize the effect of junction capacitance on the operating frequency.

The operating frequency ($f$) is given by

$$f = \frac{1}{2\pi} \times \sqrt{\frac{1}{L} \times \left\{\left[\left(\frac{1}{C_1}\right) + \left(\frac{1}{C_2}\right) + \left(\frac{1}{C_3}\right)\right]\right\}} \tag{12.46}$$

If $C_3$ is chosen to be much smaller than either $C_1$ or $C_2$, then expression for frequency ($f$) simplifies to

$$f = \frac{1}{2\pi\sqrt{LC_3}} \tag{12.47}$$

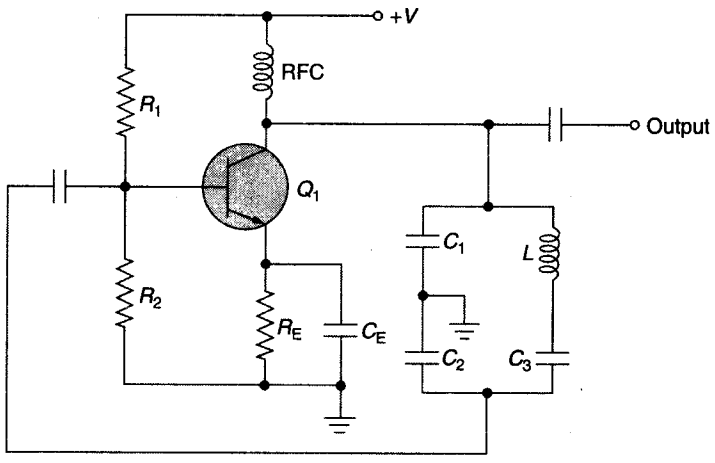



**Figure 12.30** | Clapp oscillator.

Remember that we still need $C_1$ and $C_2$ to provide the required phase shift for regenerative feedback. Clapp oscillator is preferred over Colpitt oscillator for designing variable frequency oscillators. The adjustment of tuning element ($C_3$ in Clapp oscillator) does not alter the attenuation factor in Clapp oscillator. The attenuation factor is decided by $C_1$ and $C_2$. In the case of Colpitt oscillator, any attempt to vary the frequency by varying either $C_1$ or $C_2$ might cause cessation of oscillations over a portion of desired frequency range.

**EXAMPLE 12.10**

*Refer to the Armstrong oscillator circuit of Figure 12.31. Determine (a) frequency of oscillations and (b) minimum amplifier gain required to start oscillations. How would the oscillation frequency change if the loaded Q-factor of the tank circuit were given to be 5?*

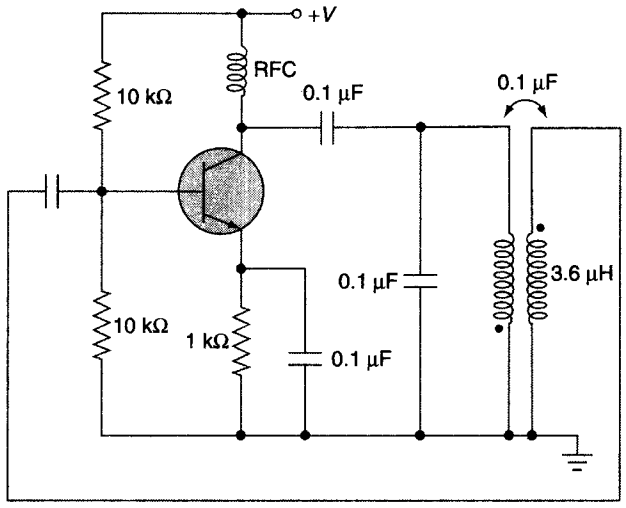



**Figure 12.31** | Example 12.10.

**Solution**

1. Frequency of oscillations, $f = 1/2\pi\sqrt{LC} = 1/(6.283\sqrt{3.6\times10^{-6}\times0.1\times10^{-6}}) = 265.3$ kHz.
2. Feedback factor = $0.1 \times 10^{-6}/3.6 \times 10^{-6} = 1/36$.
3. Therefore, minimum value of amplifier gain required to start oscillations = 36.
4. $Q$-factor of the tank circuit = 5.
5. Frequency of oscillation will reduce by a factor equal to $\sqrt{Q^2/(Q^2+1)}$.
6. Therefore, new frequency of oscillations will be $265.3 \times 10^3 \times \sqrt{5^2/(5^2+1)} = 260.1$ kHz.

**EXAMPLE 12.11**

*Refer to the Colpitt oscillator of Figure 12.32. Determine (a) frequency of oscillations and (b) minimum gain required to start oscillations.*

**Solution**

1. Equivalent value of capacitance, $C$, in the tank circuit
   $C = 0.1 \times 10^{-6} \times 0.01 \times 10^{-6}/(0.1 \times 10^{-6} + 0.01 \times 10^{-6}) = 0.009$ μF
2. Inductance, $L = 10$ μH.

3. Therefore, frequency of oscillations, $f = 1/(2\pi\sqrt{10\times10^{-6}\times0.009\times10^{-6}}) = 530.5$ kHz.
4. Feedback factor = $0.01 \times 10^{-6}/0.1 \times 10^{-6} = 1/10$.
5. Therefore, minimum value of amplifier gain = 10.

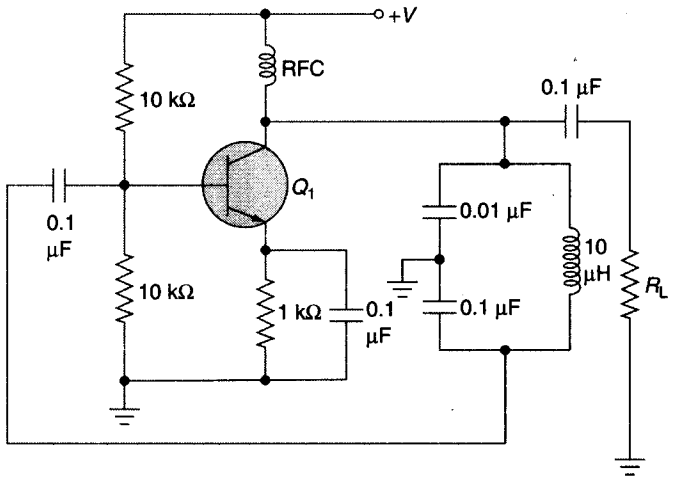



**Figure 12.32** | Example 12.11.

**EXAMPLE 12.12**

*Refer to the Hartley oscillator of Figure 12.33. Determine (a) operating frequency and (b) maximum acceptable value of resistance (R) for oscillations to start.*

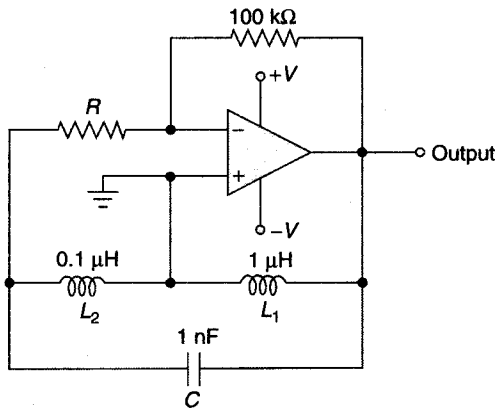



**Figure 12.33** | Example 12.12.

**Solution**

1. Frequency of oscillations is given by $f = 1/2\pi\sqrt{LC}$.
2. $L = L_1 + L_2 = 1.0 \times 10^{-6} + 0.1 \times 10^{-6} = 1.1$ μH and $C = 1$ nF.

3. Therefore, $f = 1/(6.283 \times \sqrt{1.1 \times 10^{-6} \times 1 \times 10^{-9}}) = 4.799$ MHz.
4. Feedback factor = $(0.1 \times 10^{-6})/(1.0 \times 10^{-6}) = 0.1$.
5. Therefore, minimum required gain = 10.
6. Now, |gain| = $100 \times 10^3/R$.
7. Therefore maximum value of $R = 10^5/10 = 10^4\ \Omega = 10\ k\Omega$.

**EXAMPLE 12.13**

*Refer to the Colpitt oscillator of Figure 12.32. The circuit is slightly modified by connecting an additional capacitor of 1.0 nF in series with the inductance (L) as shown in Figure 12.34. Does the modified oscillator configuration resemble any standard oscillator configuration? Determine frequency of oscillations in this case.*

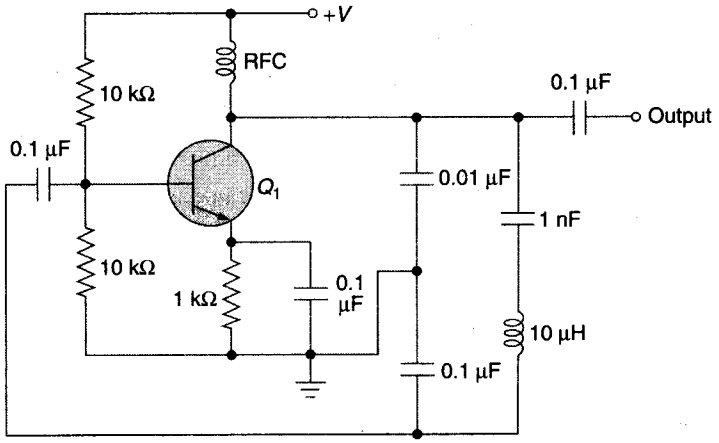



**Figure 12.34** | Example 12.13.

**Solution**

1. The modified circuit is the Clapp oscillator configuration.
2. The frequency of oscillations is given by $f = 1/2\pi\sqrt{LC}$.
3. In the present case, $C$, is given by $1/C = (1/C_1) + (1/C_2) + (1/C_3)$.
4. Substituting for $C_1$, $C_2$ and $C_3$, we get $1/C = 1/(0.01 \times 10^{-6}) + 1/(0.1 \times 10^{-6}) + 1/(1 \times 10^{-9})$.
5. This gives $C = 0.0009$ μF.
6. Therefore, $f = 1/(6.283 \times \sqrt{10 \times 10^{-6} \times 0.0009 \times 10^{-6}}) = 1.677$ MHz.

**EXAMPLE 12.14**

*Refer to the oscillator of Figure 12.35. Does the given oscillator circuit resemble any standard oscillator configuration? If yes, identify the oscillator configuration. Also, determine its frequency of oscillations and the required minimum value of amplifier gain.*

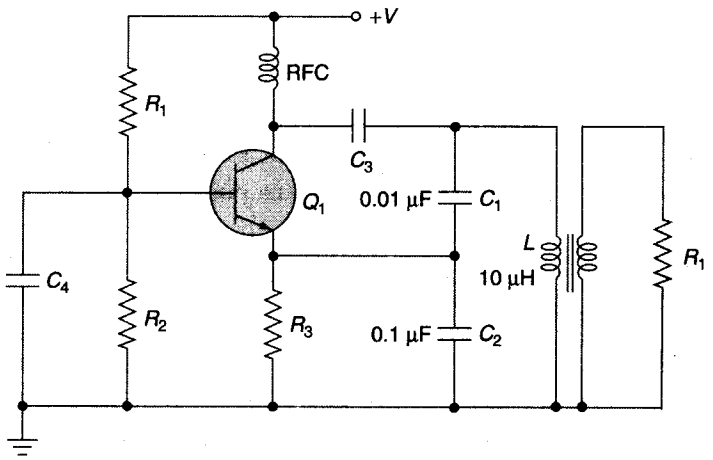



**Figure 12.35** | Example 12.14.

**Solution**

1. If we carefully examine the given circuit, we find that it follows the Colpitt oscillator configuration.
2. The feedback circuit in this case is also a tank circuit comprising a pair of series connected capacitors $C_1$ and $C_2$ and an inductor $L$.
3. Also, the amplifier has been wired in common-base configuration. Note that the base terminal is effectively grounded for AC signal through capacitor $C_4$.
4. The output in this case appears across series combination of $C_1$ and $C_2$. It appeared across $C_1$ only in the case of Colpitt oscillator configured around common-emitter amplifier. The feedback signal appears across $C_2$ in both the cases.
5. The feedback factor in this case is therefore given by $[C_1 \times C_2/(C_1 + C_2)]/C_2$, which simplifies to $C_1/(C_1 + C_2)$.
6. The required minimum value of amplifier gain is therefore $(C_1 + C_2)/C_1$.
7. Frequency of oscillations can be computed from $f = 1/2\pi\sqrt{LC}$, where $C = C_1 \times C_2/(C_1 + C_2)$.
8. Now $C = 0.01 \times 10^{-6} \times 0.1 \times 10^{-6}/(0.01 \times 10^{-6} + 0.1 \times 10^{-6}) = 0.009$ μF.
9. Therefore, $f = 1/2\pi\sqrt{10 \times 10^{-6} \times 0.009 \times 10^{-6}} = 530.5$ kHz.
10. Feedback factor $= 0.01 \times 10^{-6}/(0.01 \times 10^{-6} + 0.1 \times 10^{-6}) = 1/11$.
11. Also, required minimum value of amplifier gain = 11.

## 12.15 Crystal Oscillator

In the case of a crystal oscillator, a quartz crystal with the desired value of resonant frequency forms part of the frequency-selective feedback network. Crystal oscillator is the natural choice when the accuracy and stability of oscillation frequency is of paramount importance. In order to understand the operation of crystal oscillators, it is important that we first study and analyze the AC equivalent circuit of the crystal as a component.

## AC Equivalent Circuit of a Quartz Crystal

Figure 12.36 shows the circuit representation and AC equivalent circuit of the quartz crystal. $R$, $L$ and $C_S$, respectively, represent the resistance, inductance and capacitance of the piezoelectric crystal element. $C_M$ represents the mounting capacitance. It is in fact the capacitance due to the parallel-plate capacitor formed by the connecting electrodes and the piezoelectric element constituting the dielectric. Typically, $R$ is in the range of few hundreds of ohms to a few kilo-ohms; $L$ is of the order of few tens of milli-henries to few henries, $C_S$ is a very small fraction of a pico-farad and $C_M$ is few pico-farads. The $Q$-factor of the crystal is given by $Q = \omega L/R = 1/\omega C_S R$.

The crystal exhibits two resonant frequencies. One is the series resonant frequency $f_S$. It is the frequency at which the inductive reactance of inductance $L$ equals the capacitive reactance of capacitance $C_S$. It is expressed as

$$f_S = \frac{1}{2\pi\sqrt{LC_S}} \tag{12.48}$$

Figure 12.37 shows the plot of reactance versus frequency for the equivalent circuit of Figure 12.36. Quite understandably, the impedance is a capacitive reactance below the series resonant frequency and an

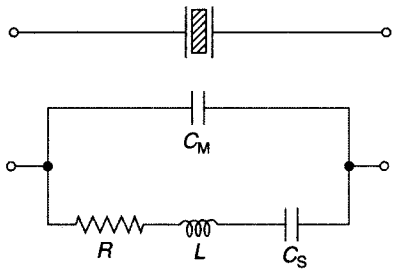



**Figure 12.36** | Circuit representation and AC equivalent circuit of a quartz crystal.

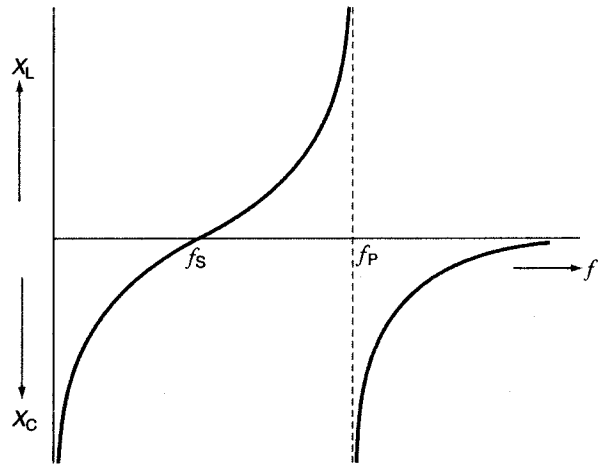



**Figure 12.37** | Reactance versus frequency plot of a quartz crystal.

inductive reactance above it. The second resonant frequency called the parallel resonant frequency ($f_P$) occurs at a value where the inductive reactance equals the capacitive reactance due to equivalent capacitance of the tank circuit. Parallel resonance occurs at a frequency where the circulating loop current is at its maximum. Since circulating loop current flows through series combination of $C_S$ and $C_M$, therefore the equivalent capacitance of the parallel tuned circuit is given by

$$C_P = \frac{C_M \times C_S}{C_M + C_S} \tag{12.49}$$

Parallel resonant frequency is given by

$$f_P = \frac{1}{2\pi\sqrt{LC_P}} \tag{12.50}$$

Since $C_S$ is much smaller than $C_M$, $C_P$ is only marginally less than $C_S$ with the result that $f_S$ and $f_P$ are very close to each other. The apparent difference between $f_S$ and $f_P$ as shown in Figure 12.37 is an exaggerated one to explain the operation of the crystal.

The two resonant frequencies described in the previous paragraph are the fundamental resonant frequencies. Remember that the specified crystal frequency is between $f_S$ and $f_P$. This area of frequencies between $f_S$ and $f_P$ is known as the area of usual parallel resonance or simply the area of parallel resonance. A crystal can also resonate at harmonics of the fundamental frequency called overtones. The fundamental resonant frequency of the crystal is usually limited to less than 30 MHz due to the smallest physical dimension the crystal can be cut to. Operation in the overtone mode allows stable output at much higher frequencies.

## Extremely High Frequency Stability

The extremely high frequency stability of a crystal oscillator comes from its extremely stable values of inductance and capacitance and a very high value of its $Q$-factor. Remember that the oscillation frequency of an $LC$ oscillator in addition to the values of $L$ and $C$ also depends upon the $Q$-factor of the $LC$ circuit. The generalized expression is given by

$$f = [1/(2\pi\sqrt{LC})] \times \sqrt{Q^2/(Q^2+1)} \tag{12.51}$$

A very high value of $Q$-factor in the case of quartz crystal ensures that the stability of oscillation frequency exclusively depends upon the operational stability of crystal elements. As a component, crystal is extremely stable.

A high value of $Q$-factor also produces a high value of rate of change of phase with respect to frequency ($d\theta/d\omega$), where $\theta$ represents phase. It implies that even infinitesimally small change in $\omega$ will produce a sufficient change in $\theta$ to restore the frequency to the original value. In general, the frequency-determining network of an oscillator should be made up of elements with extremely high operational stability and its Q-factor should be high. On both these accounts, quartz crystal has no competitor. It has $Q$-factor approaching tens of thousands and as a component, it is extremely stable.

## Crystal Oscillator Circuits

As is evident from the impedance versus frequency characteristics of a crystal, depending upon the circuit characteristics, it can act like a capacitor, an inductor, a series-tuned circuit or a parallel-tuned circuit. There are a large number of crystal oscillator configurations depending upon the mode in which the crystal is used. In one of the categories of crystal oscillator, crystal is connected in series with the $LC$ tank circuit in the feedback path. Each of the $LC$ oscillator circuits discussed in Section 12.14 (Armstrong, Hartley, Colpitt and Clapp) can be configured as a crystal-controlled oscillator by connecting a crystal in series with the tank circuit.

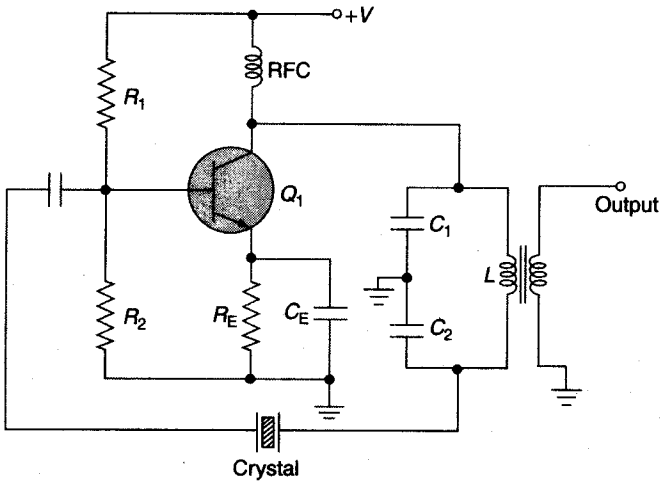



**Figure 12.38** | Crystal-controlled Colpitt oscillator.

Figure 12.38 shows one such oscillator circuit. It is the modified Colpitt oscillator circuit. The circuit operates as follows. The *LC* tank circuit is tuned to the series resonant frequency of the crystal. The crystal offers minimum impedance at the series resonant frequency and thus allows the feedback signal to reach the input with practically no additional attenuation. A slight variation in frequency introduces very high impedance. The feedback signal is further attenuated to an extent that loop gain criterion is not met and the oscillations stop. Thus the oscillator can oscillate only at the resonant frequency of the crystal, thus significantly improving the frequency stability of the oscillator. Armstrong, Hartley and Clapp oscillator circuits can similarly be modified by introducing a quartz crystal in series with the respective tank circuits.

Figure 12.39 shows another variation of crystal-controlled Colpitt oscillator circuit. Here crystal forms a part of the tank circuit. The crystal acts like an inductor that resonates with capacitors $C_1$ and $C_2$. The resonant frequency is somewhere between the series and parallel resonant frequencies of the quartz crystal.

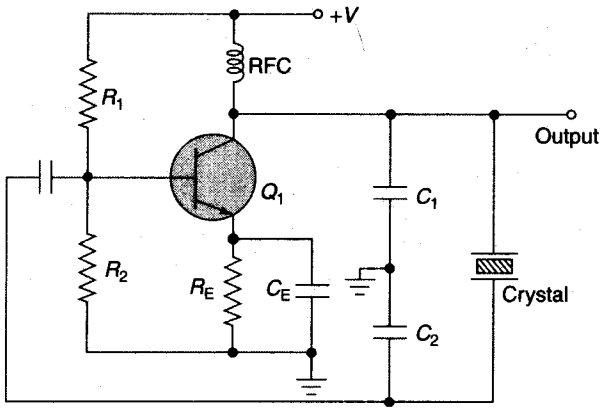



**Figure 12.39** | Crystal-based Colpitt oscillator with common-emitter amplifier.

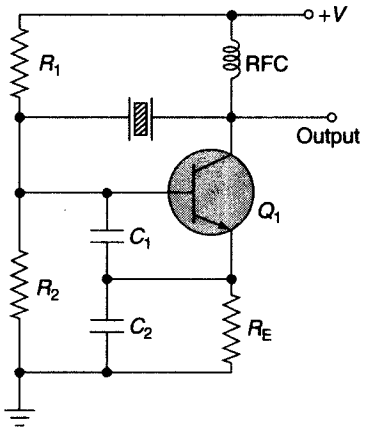



**Figure 12.40** | Crystal-based Colpitt oscillator with common-base amplifier.

Figure 12.40 shows a slightly modified Colpitt oscillator circuit that uses common-base amplifier configuration instead of common-emitter configuration used in the oscillator circuit of Figure 12.39. Common-base amplifier configuration allows operation at relatively higher oscillation frequencies.

Yet another application of Colpitt oscillator configuration is found in what is popularly known as *Pierce oscillator*. Figure 12.41 shows the basic circuit implementation of a Pierce oscillator. An FET (JFET or MOSFET) is used as the active device and the crystal along with the inter-electrode capacitances $C_{gs}$ and $C_{ds}$ constitute the feedback network. Pierce oscillator of Figure 12.41 is redrawn in Figure 12.42 to demonstrate its resemblance to Colpitt oscillator configuration. The oscillation frequency is the parallel resonant frequency of the crystal and the inter-electrode capacitances do not play any role in determining oscillation frequency. The feedback factor and therefore the required amplifier gain are determined by $C_{gs}$ and $C_{ds}$. In fact, it is observed that the oscillator stops oscillating as the oscillation frequency is reduced to below about 2 MHz due to insufficient feedback. In a situation like this, it becomes imperative to have external capacitors between gate-source and drain-source terminals. Pierce oscillator works very well in very high frequency (VHF) and ultra high frequency (UHF) frequency ranges. Purpose of putting radio-frequency choke (RFC) is to prevent the high-frequency output from getting grounded through drain power supply.

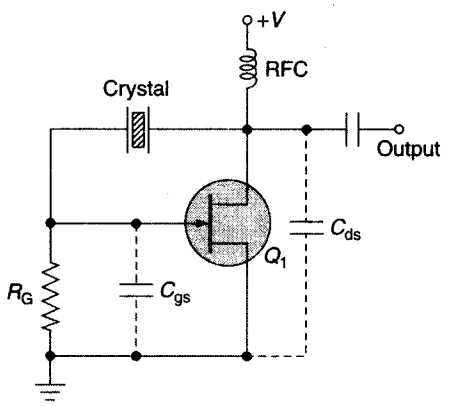



**Figure 12.41** | Basic Pierce oscillator.

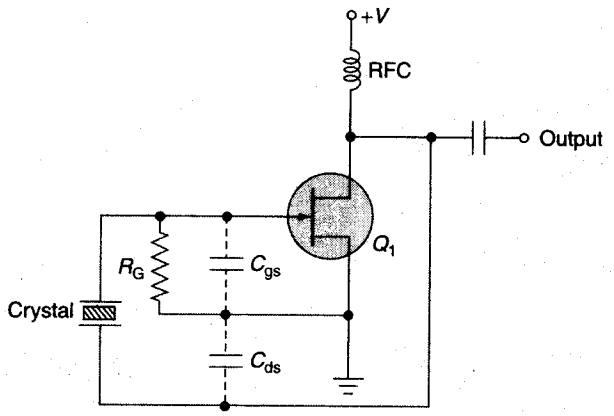



**Figure 12.42** | Basic Pierce oscillator

**EXAMPLE 12.15**

*A quartz crystal is characterized by L = 2.5 H, R = 1 kΩ, $C_S$ = 0.01 pF and $C_M$ = 10 pF. Determine the series and parallel resonant frequencies of the crystal.*

**Solution**

1. Series resonant frequency, $f_S = 1/2\pi\sqrt{LC_S} = 1/(6.283\sqrt{2.5\times0.01\times10^{-12}}$ = 1.006614 MHz.
2. Equivalent capacitance $C_P$ for the parallel resonant circuit
   $C_P = 0.01 \times 10^{-12} \times 10 \times 10^{-12}/(0.01 \times 10^{-12} + 10 \times 10^{-12})$ pF = 0.00999 pF
3. Parallel resonant frequency, $f_P = 1/2\pi\sqrt{LC_P}$.
4. Substituting the values, we get $f_P = 1/(6.283\sqrt{2.5\times0.00999\times10^{-12}})$ = 1.007117 MHz.

## 12.16 Voltage-Controlled Oscillators

A voltage-controlled oscillator (VCO) is an oscillator circuit in which the frequency of oscillations can be varied by an applied DC control voltage. This is achieved by having a voltage-dependent capacitor commonly known as varicap or a varactor diode as a part of the frequency-determining tank circuit.

Hartley and Clapp oscillator configurations are particularly suited to building VCOs as in both cases, the frequency-determining *LC* circuit has a single capacitor and tuning can be easily done by replacing this capacitor by a varactor diode. Figure 12.43 shows the basic voltage-controlled Hartley oscillator configured around a junction FET. A similar circuit could be configured around a bipolar transistor also. In the circuit shown in Figure 12.43, the amplifier is configured as common-drain amplifier with voltage gain slightly less than unity. In this case, the feedback factor is greater than one as the output signal appears across portion of the coil between source terminal and ground and the feedback signal appears across the whole of the coil winding.

Use of a single varactor diode is usually discouraged. This is because of the reason that for small values of DC control voltages, the varactor diode may start conducting at either of the peaks of the RF signal depending upon how it is connected in the circuit. Conducting diode reduces the Q-factor of the tank circuit and deteriorates the phase noise performance. Back-to-back connection of two varactor diodes overcomes this problem.

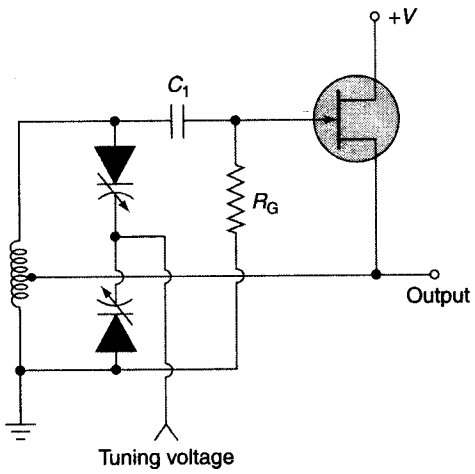



**Figure 12.43** | Voltage-controlled Hartley oscillator.

Another application of VCO is in fine tuning of crystal oscillators. The oscillator frequency may be varied by few tens of parts per million as the high value of $Q$-factor in the case of crystals allows pulling only over a small range. Fine tuning of crystal oscillator frequency may be needed to adjust output frequency to either match or be an exact multiple of some external reference. Voltage-controlled fine tuning of crystal oscillators may also be employed in temperature-compensated VCOs (TCVCXO) to correct the temperature dependence of oscillator frequency.

## 12.17 Frequency Stability

Frequency stability of an oscillator is a measure of its ability to maintain a constant oscillation frequency for as long a time period as possible. The oscillation frequency depends upon a large number of circuit features, which include circuit components, stray elements, supply voltages, characteristic parameters of active devices and so on. While one could pay due attention to choice of circuit components, use of clean and regulated supply voltages, etc., it may not be practical to identify location and estimation of magnitude of stray capacitances and inductances. This implies that it would be extremely hard to take remedial measures to counter the frequency drift caused by these elements. Equally impractical would be neutralizing the ill effects of instability of characteristic parameters of active devices.

Fortunately though, not all circuit features influence the oscillation frequency to the same extent. Oscillation frequency is usually far more sensitive to variation in a small number of circuit features than it is to the large number of remaining circuit features. For example, in the case of RC phase shift and Wien bridge oscillator circuits, frequency stability is largely dependent upon stability of $R$ and $C$. Similarly, in an $LC$ oscillator, it would mainly depend upon stability of $L$ and $C$.

### *Frequency Stability Criterion*

According to the frequency stability criterion, if there exists a small set of elements which introduces a large phase change ($d\theta$) for a given change in frequency ($d\omega$), then higher the value of $d\theta/d\omega$, more will be the dependence of $\omega$ on this set of elements as compared to its dependence on other circuit features. In the limit when $d\theta/d\omega$ approaches infinity; $\omega$ becomes independent of all other features and depends only on this small set of elements.

It can also be argued that $d\theta/d\omega$ is a measure of frequency stability of the oscillator and a higher value of $d\theta/d\omega$ means higher frequency stability. The argument goes as follows. Let us assume that one of the circuit features other than one of the elements of the small set mentioned above undergoes a variation. As a consequence of this variation, if the loop phase shift criterion were earlier satisfied at the operational frequency, it would no longer be satisfied after the variation takes place. The operational frequency must therefore shift in order to restore the loop phase shift back to zero. But if there were a small set of elements which at the nominal oscillation frequency produced a large change in phase for a given change in frequency, then the required frequency change to restore the loop phase shift condition would also be very small. This, in other words, means that the oscillator exhibits a high level of frequency stability.

This concept can be used to explain relatively higher frequency stability of *LC* oscillators in general, which improves with increase in the value of the *Q*-factor of the *LC* resonant circuit. It can similarly be used to explain the exceptionally high-frequency stability of crystal oscillators. In the case of *LC* oscillators, the reactance changes from capacitive to inductive around the frequency of resonance. Higher the *Q*-factor of the *LC* circuit, more abrupt is this change of phase. This further implies that higher *Q*-factor leads to a higher $d\theta/d\omega$ and consequently higher frequency stability. The frequency stability can be quantified by computing the magnitude of $d\theta/d\omega$ at the nominal oscillation frequency by differentiating the expression for the phase angle for the transfer function of the feedback network with respect to $\omega$.

**EXAMPLE 12.16**

*Derive the relevant expression to prove that the Wien bridge oscillator exhibits better frequency stability at relatively lower oscillation frequencies and that the frequency stability deteriorates with increase in oscillation frequency.*

**Solution**

1. The expression for phase angle ($\theta$) as a function of frequency ($\omega$) in the case of Wien bridge oscillator can be written as $\theta = 90° - \tan^{-1}[3\omega RC/(1 - \omega^2R^2C^2)]$. This equation is obtained by substituting $R_1 = R_2 = R$ and $C_1 = C_2 = C$ in Eq. (12.36).
2. The above equation can also be written as $\theta = \tan^{-1}[(1 - \omega^2R^2C^2)/3\omega RC]$.
3. In general $(d/dx)(\tan^{-1}u) = [1/(1 + u^2)] \times du/dx$.
4. Using this formula, $d\theta/d\omega = KRC$, where $K$ is a constant.
5. The above expression implies that product RC needs to have a higher value in order to have higher $d\theta/d\omega$ and therefore higher stability.
6. Higher RC means lower operating frequency.
7. This proves that the Wien bridge oscillator exhibits better frequency stability at lower oscillation frequencies and that the frequency stability deteriorates as the frequency of oscillation increases.

## KEY TERMS

Armstrong oscillator
Barkhausen criterion
Bubba oscillator
Buffered RC phase shift oscillator
Clapp oscillator
Colpitt oscillator
Crystal oscillator
Frequency stability

Hartley oscillator
LC oscillators
Meissner oscillator
Pierce oscillator
Quadrature oscillator
RC oscillators
RC phase shift oscillator
Series-fed LC oscillator
Shunt-fed LC oscillator
Tickler coil
Tickler oscillator
Twin-T oscillator
Wien bridge oscillator
Voltage-controlled oscillator

## OBJECTIVE-TYPE EXERCISES

### *Multiple-Choice Questions*

1. According to Barkhausen criterion for sustained oscillations,
   **a.** $\beta A < 1$.
   **b.** $\beta A > 1$.
   **c.** $\beta A = 1$.
   **d.** $\beta A = 0$.
2. The condition that decides the oscillator's output frequency is
   **a.** loop gain should at least be unity.
   **b.** loop phase shift should be zero or integral multiple of $2\pi$ radians.
   **c.** loop gain should be precisely unity.
   **d.** loop phase shift should be precisely zero radian.
3. In a conventional transistor RC phase shift oscillator using lead-type feedback network, frequency of oscillations is given by
   **a.** $f = \frac{1}{2\pi RC}$
   **b.** $f = \frac{1}{2\pi\sqrt{RC}}$
   **c.** $f = \frac{1}{2\pi\sqrt{6}RC}$
   **d.** $f = \frac{1}{2\pi\sqrt{3}RC}$
4. In a Wien bridge oscillator, frequency of oscillations is given by
   **a.** $f = \frac{1}{2\pi RC}$
   **b.** $f = \frac{1}{RC}$
   **c.** $f = \frac{1}{2\pi\sqrt{6}RC}$
   **d.** $f = \frac{1}{2\pi\sqrt{3}RC}$
5. Most popular oscillator configuration for audio applications is
   **a.** Hartley oscillator.
   **b.** Colpitt oscillator.
   **c.** Wien bridge oscillator.
   **d.** RC phase shift oscillator.
6. Which of the following oscillator types provides extremely stable output frequency?
   **a.** Hartley oscillator.
   **b.** Wien bridge oscillator.
   **c.** Crystal oscillator.
   **d.** Clapp oscillator.
7. Pick the odd-one out.
   **a.** Hartley oscillator.
   **b.** Colpitt oscillator.
   **c.** Clapp oscillator.
   **d.** Wien bridge oscillator.
8. Of the following, the oscillator with the most stable oscillation frequency is
   **a.** Clapp oscillator.
   **b.** Colpitt oscillator.
   **c.** Hartley oscillator.
   **d.** Armstrong oscillator.
9. The series and parallel resonant frequencies of a quartz crystal are
   **a.** the same.
   **b.** spaced far apart.
   **c.** very close to each other.
   **d.** in the range of tens of MHz.
10. The feedback network of a conventional RC phase shift oscillator uses

a. three lag-type RC sections.
b. three lead-type RC sections.
c. three RC sections of either lead or lag type.
d. twin-T notch filter.

11. In the case of a buffered RC phase shift RC oscillator, the required minimum value of amplifier gain is
a. 29.
b. 8.
c. 3.
d. 16.

12. According to the frequency stability criterion,
a. higher $|d\theta/d\omega|$ means higher frequency stability.
b. higher $|d\theta/d\omega|$ means lower frequency stability.
c. frequency stability is independent of $|d\theta/d\omega|$.
d. higher value of $Q$-factor means lower frequency stability.

## *Identify the Oscillator Configuration*

Identify the oscillator circuits of Figure 12.44. Choose from Hartley oscillator, Colpitt oscillator, Clapp oscillator, Tickler oscillator, Pierce oscillator, Wien bridge oscillator, RC phase shift oscillator, Crystal oscillator, Bubba oscillator and Twin-T oscillator.

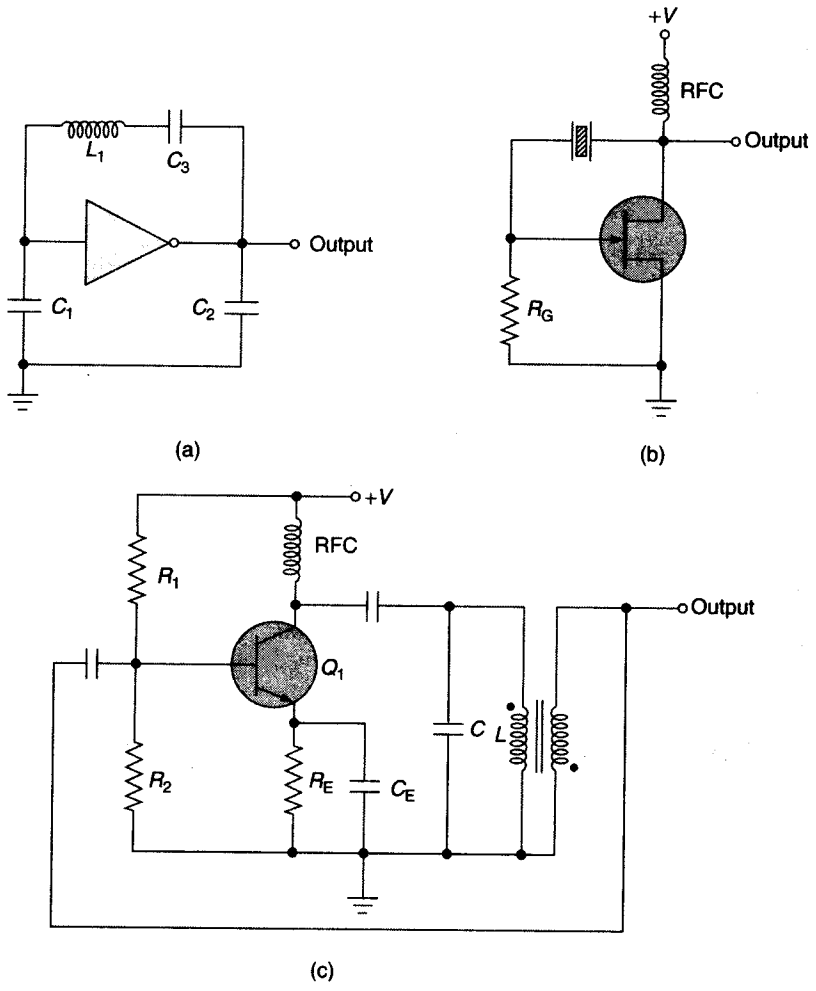
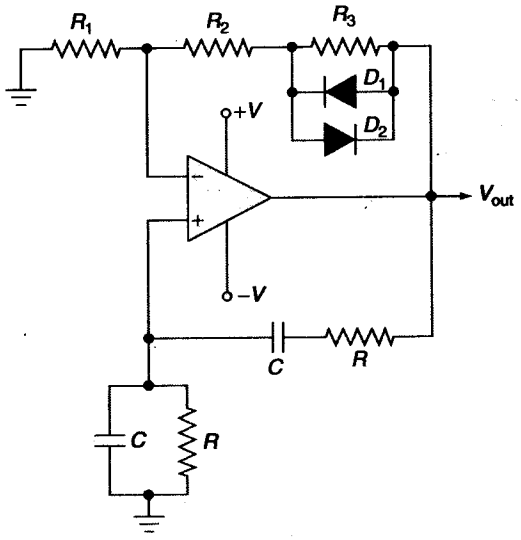
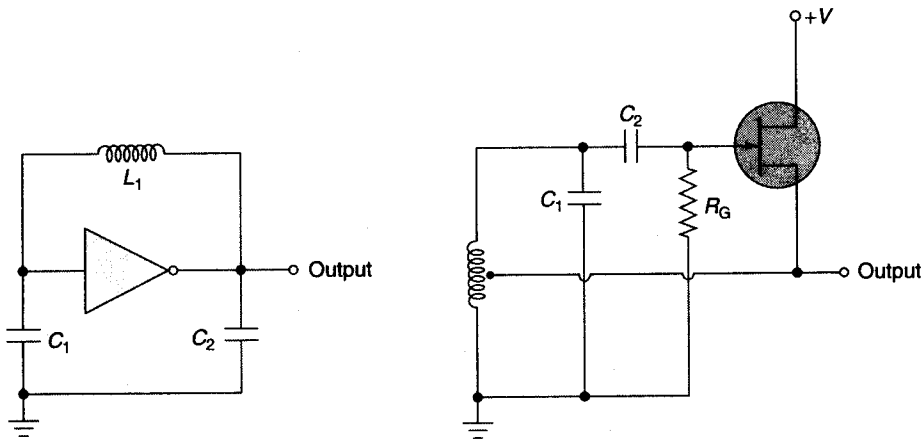



**Figure 12.44** | Identify the oscillator configuration.




(d)




(e) (f)

**Figure 12.44** | *Continued.*

## REVIEW QUESTIONS

1. How does the circuit configuration of an oscillator differ from that of an amplifier? What are the different constituents of an oscillator circuit?
2. What are the necessary conditions of loop gain and loop phase shift for sustained oscillations according to Barkhausen criterion? Why is the loop gain in practical oscillators kept slightly greater than unity?
3. With the help of relevant circuit diagram, briefly describe the operation of an RC phase shift

oscillator configured around an opamp and a lead-type feedback network. What should be the minimum value of amplifier gain for sustained oscillations? What is the phase shift introduced by each of the three RC sections in the feedback network at the operating frequency?

4. Derive the expressions for the phase shift as a function of frequency for the feedback networks of RC phase shift and Wien bridge oscillators to prove that these oscillators exhibit better frequency stability at relatively lower operating frequencies.

5. What are buffered RC phase shift oscillators? How does the operating frequency in the case of a buffered oscillator differ from that of conventional non-buffered counterpart?

6. Briefly describe the operation of Quadrature oscillator with particular reference to its ability to produce sine and cosine outputs.

7. With the help of relevant circuit diagram, describe the operation of a Wien bridge oscillator configured around an opamp. What are the phase shifts introduced by the feedback and amplifier parts? Derive the relevant expression to prove that the amplifier should have a gain of at least 3 for sustained oscillations.

8. Why are LC oscillators not suitable for relatively lower frequencies? How does the frequency stability of an LC oscillator depend upon the $Q$-factor of the LC circuit?

9. What are crystal oscillators? What makes crystal oscillator exhibit exceptionally high frequency stability?

10. With the help of basic circuit diagram, briefly describe the operation of a Pierce oscillator. How does it differ from a Colpitt oscillator?

11. What is a voltage-controlled oscillator? Why is it important to use back-to-back connected varactor diodes instead of a single diode?

12. Briefly outline the frequency stability criterion in the case of oscillators. Which parameter can be used to quantify the frequency stability and why?

## PROBLEMS

1. Figure 12.45 shows a possible RC phase shift oscillator configured around a junction FET and designed to produce a sinusoidal output at 6.5 kHz. Will this oscillator produce the output at the expected frequency? If not, why? Assume $g_m = 5000$ μmhos and $r_d = 10$ kΩ for the junction FET.

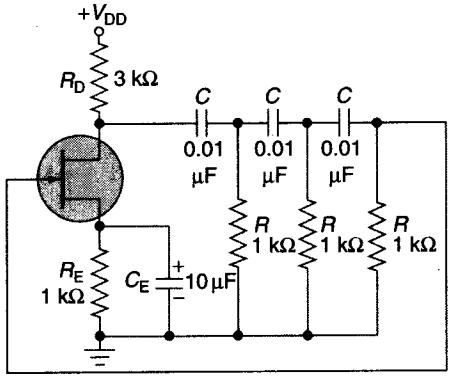



**Figure 12.45** | Problem 1.

2. Refer to the Wien bridge oscillator circuit of Figure 12.46. Determine different component values for this oscillator to produce a sine wave output at 10 kHz.

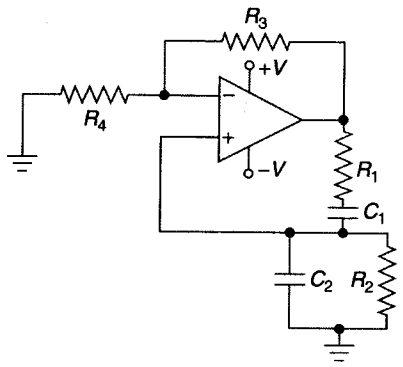



**Figure 12.46** | Problem 2.

3. Derive an expression to prove that in the case of a buffered RC phase shift oscillator using a lag-type feedback network, $|d\theta/d\omega|$ equals $RC/4$.

4. Refer to the Hartley oscillator circuit of Figure 12.47. Determine the oscillation frequency. Also determine the minimum value of $R_1$ for sustained oscillations.

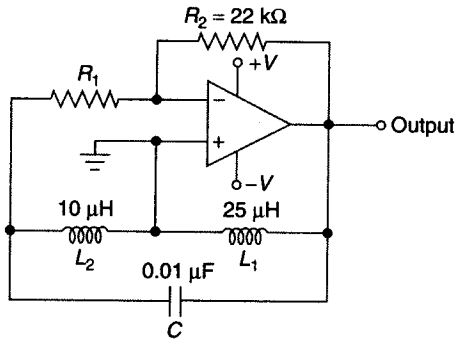



**Figure 12.47** | Problem 4.

5. Refer to the Colpitt oscillator circuit of Figure 12.48. Determine the oscillation frequency. Also determine the minimum value of $R_1$ for sustained oscillations.

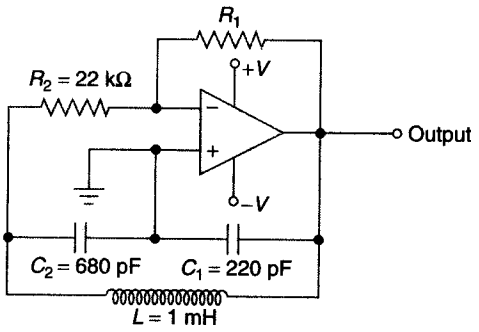



**Figure 12.48** | Problem 5.

6. An LC oscillator is observed to produce sine wave output at 10 MHz when the $Q$-factor of the LC circuit was 100. How would the operating frequency change if at all it would with the $Q$-factor dropping to 10?

7. Determine the minimum amplifier gain and the phase shift required to be introduced by the amplifier for the following cases.
   a. Feedback factor = 2%, oscillator type = Hartley oscillator
   b. Feedback factor = 5%, oscillator type = Wien bridge oscillator

8. A conventional RC phase shift oscillator operates at a frequency of 10 kHz. How would its operating frequency change if different RC sections were buffered and the feedback network used lead-type RC sections?

9. Refer to the RC oscillator of Figure 12.49. Determine oscillation frequency.

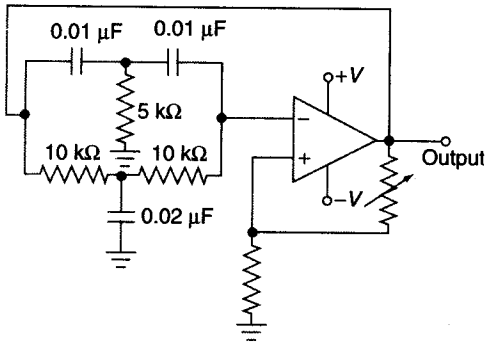



**Figure 12.49** | Problem 9.

**10.** A quartz crystal is characterized by series resistance, inductance and capacitance of 1000 Ω, 3 H and 0.05 pF, respectively. The mounting capacitance of the crystal is 10 pF. Determine (a) series resonant frequency of the crystal; (b) parallel resonant frequency of the crystal and (c) operating frequency of the oscillator using this crystal in Pierce oscillator configuration.

# ANSWERS

## Multiple-Choice Questions

**1.** (c)
**2.** (b)
**3.** (c)
**4.** (a)
**5.** (c)
**6.** (c)
**7.** (d)
**8.** (a)
**9.** (c)
**10.** (c)
**11.** (b)
**12.** (a)

## Identify the Oscillator Configuration

Figure 12.44(a): Clapp oscillator
Figure 12.44(b): Pierce oscillator
Figure 12.44(c): Tickler oscillator
Figure 12.44(d): Wien bridge oscillator
Figure 12.44(e): Colpitt oscillator
Figure 12.44(f): Hartley oscillator

## Problems

**1.** No, the gain criterion is not satisfied

**2.** $R_1 = R_2 = 1.59$ kΩ, $C_1 = C_2 = 0.01$ μF, $R_3 = 20$ kΩ, $R_4 = 10$ kΩ

**4.** $f = 269$ kHz, $R_1 = 8.8$ kΩ

**5.** $f = 390.4$ kHz, $R_1 = 68$ kΩ

**6.** 9.95 MHz

**7.** (a) Amplifier gain = 50, phase shift = 180°
(b) Amplifier gain = 20, phase shift = 0°

**8.** 14.14 kHz

**9.** 1.592 kHz

**10.** (a) 411 kHz; (b) 412 kHz; (c) 412 kHz

CHAPTER 13

# Wave-Shaping Circuits

## Learning Objectives

After completing this chapter, you will learn the following:

- RC and RL low-pass and high-pass circuits.
- RC and RL integrator and differentiator circuits.
- Different types of diode-based clipping circuits.
- Basic clamping circuit, its limitations and practical clamping circuit.
- Bistable, monostable and astable multivibrator circuits configured around discrete semiconductor devices.
- Schmitt trigger circuit and its applications.
- Multivibrator circuits configured around digital integrated circuits.
- Multivibrator circuits configured around timer IC 555.

The topics discussed in this chapter include basic linear and non-linear wave shaping circuits like the RC and RL integrator, RC and RL differentiator, clipping circuits, clamping circuits and multivibrator circuits. Though a clamping circuit is not a wave-shaping circuit in the true sense, it has been chosen to be discussed here because the concepts relevant to the operation of clamping circuits are similar to those that explain the operation of RC wave-shaping and clipping circuits. A clamper circuit acts on an AC waveform, sinusoidal or non-sinusoidal, and gives it a DC level though it does not alter the wave shape. It is an important building block of voltage-multiplying circuits. Keeping in view the scope of the present text, a separate chapter on clamping circuits would not be justified.

## 13.1 Basic RC Low-Pass Circuit

Figure 13.1 shows the basic RC low-pass circuit comprising a single-section RC circuit with output taken across the capacitor. The output voltage is given by

$$V_o = \left( \frac{X_C}{\sqrt{R^2 + X_C{}^2}} \right) \times V_i \tag{13.1}$$

Qualitatively, since the output is taken across the capacitor and the reactance of a capacitor is inversely proportional to the frequency, the output voltage will fall with increase in frequency (Figure 13.2). That is how

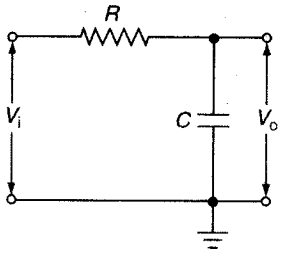



**Figure 13.1** | RC low-pass circuit.

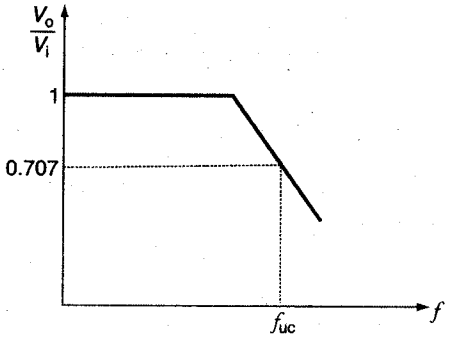



**Figure 13.2** | Frequency response of a RC low-pass circuit.

an RC network of the type shown in Figure 13.1 behaves as a low-pass circuit. The upper 3 dB cut-off frequency is the frequency at which output amplitude is 0.707 times (or 3 dB below) the nominal maximum amplitude. The nominal maximum output amplitude is same as the input amplitude; therefore, the ratio ($V_o/V_i$) equals 0.707 at 3 dB cut-off frequency.

The ratio ($V_o/V_i$) becomes 0.707 when the resistance ($R$) equals capacitive reactance ($X_C$). Therefore, the cut-off frequency ($f_{uc}$) is given by

$$f_{uc} = \frac{1}{2\pi RC} \tag{13.2}$$

We will now study the behavior of this circuit toward step and pulse inputs.

## Step Input

For a step input ($V_i$) of Figure 13.3(a), the output voltage ($V_o$), which is also voltage across $C$, rises exponentially towards the final value of $V$ with a time constant ($RC$). The output voltage ($V_o$) is given by

$$V_o = V(1 - e^{-t/RC}) \tag{13.3}$$

This expression is valid only when the capacitor is initially fully discharged. If the capacitor were initially charged to a voltage $V_o$, less than $V$, then the exponential charging equation would be

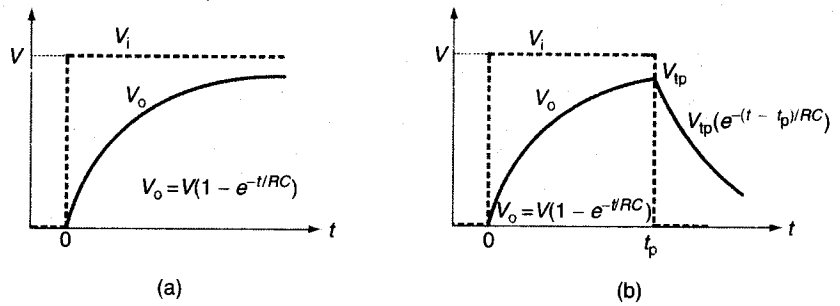



**Figure 13.3** | (a) Step response of low-pass circuit; (b) pulse response of low-pass circuit.

$$V_o = V - (V - V_o)e^{-t/RC} \tag{13.4}$$

If this input step occurs at time $t = t_1$, then the following equation represents the charging process:

$$V_o = V[1 - e^{-(t - t_1)/RC}] \tag{13.5}$$

### *Pulse Input*

For the pulse input of Figure 13.3(b), output ($V_o$) during the high time of the pulse is given by

$$V_o = V(1 - e^{-t/RC}) \tag{13.6}$$

At $t = t_p$, the amplitude of the output voltage is given by

$$V_o(t = t_p) = V(1 - e^{-t_p/RC}) = V_{tp} \tag{13.7}$$

The output ($V_o$) during the low time of the pulse is given by

$$V_o = V_{tp}(e^{-(t - t_p)/RC}) \tag{13.8}$$

We are often interested in knowing the quality with which the leading and the trailing edges will be passed through the RC low-pass circuit. Such a situation arises particularly in the analysis of high-frequency amplifiers where the amplifier input has a finite capacitance and this capacitance along with source resistance constitutes a low-pass RC network. We will see that the capability of the network to pass fast transitions depends upon the upper 3 dB cut-off frequency of the network.

The quality with which this network reproduces fast transitions is expressed by the magnitude of the rise time ($t_r$) which is the time taken by the output to change from 10% to 90% of the impressed transition or step. From the exponential charging relationship, it can be verified that

$$t_r = 2.2RC \tag{13.9}$$

The relationship between the upper 3 dB cut-off frequency ($f_{uc}$) and the rise time ($t_r$) is given by

$$f_{uc} = \frac{0.35}{t_r} \tag{13.10}$$

where $f_{uc}$ is specified in MHz and $t_r$ is specified in μs. This expression indicates that higher the upper 3 dB cut-off frequency, smaller is the rise time. Therefore, for faithful reproduction of fast transitions, $f_{uc}$ should be as high as possible.

## 13.2 RC Low-Pass Circuit as Integrator

If the circuit shown in Figure 13.1 is an integrator circuit, the output voltage $V_o$ should be integral of the input voltage ($V_i$), that is,

$$V_o = K\int V_i dt$$

where $K$ is a constant. In the given RC circuit, if the product $RC$ is much larger than the time period ($T$) of the applied input, the capacitor voltage (or the output voltage in the present case) would change by only a very small amount as the input goes through a complete cycle. In such a case, it is not wrong to assume that whole of input voltage ($V_i$) appears across the resistor ($R$) only. As a result current ($I_i$) can be expressed as

$$I_i = \frac{V_i}{R}$$

The output voltage ($V_o$) across the capacitor is given by

$$V_o = \frac{1}{C}\int I_i dt = \frac{1}{C}\int \frac{V_i}{R} dt = \frac{1}{RC}\int V_i dt \tag{13.11}$$

Therefore, output voltage ($V_o$) is integral of input voltage ($V_i$) provided that the time constant is much larger than the time period of the input signal, that is, $RC >> T$. In fact, if $RC \geq 15T$ integration is near ideal.

**EXAMPLE 13.1**

*Refer to Figure 13.4. Determine the amplitude of $V_o$ at the time of input pulse going low and also 1 ms after it has gone low.*

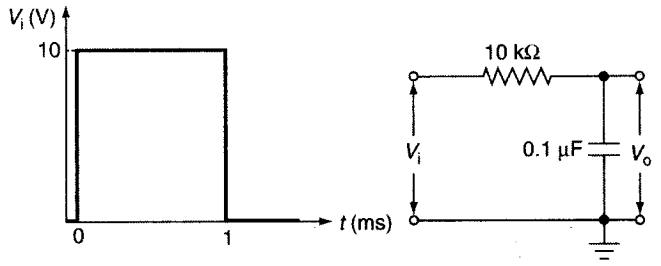



**Figure 13.4** | Example 13.1.

**Solution**

1. The time constant = $R \times C = 10 \times 10^3 \times 0.1 \times 10^{-6} = 10^{-3}$ s = 1 ms.
2. Coincidentally, the time constant equals the pulse width. The output $V_o$ will be 63.1% of the final value of 10 V, that is, $V_o$ = 6.31 V at the time of pulse going high to low.
3. In general, the charging process is governed by the expression

$$V_o = V(1 - e^{-t/RC})$$

For $t$ = RC, output voltage $V_o$ is 63.1% of the final voltage ($V$).

4. When the input pulse goes low, the capacitor starts discharging as per

$$V_o = V'(e^{-(t-t_p)/RC})$$

Here, $V'$ = 6.31 V and $t_p$ = 1 ms. Again $V_o$ will be 36.9% of ($V'$) 1 ms after the capacitor starts discharging as 1 ms happens to be equal to circuit time constant. Therefore, the output voltage after 1 ms = 0.369 × 6.31 V = 2.33 V.

5. The output waveform is shown in Figure 13.5.

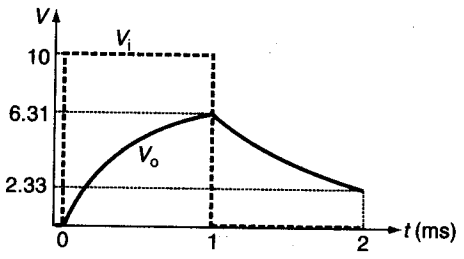



**Figure 13.5** | Solution to Example 13.1.

**EXAMPLE 13.2**

*How will the circuit of Figure 13.6(a) respond to a 10 V step input of Figure 13.6(b)? In what time will the output rise from 1 V to 9 V?*

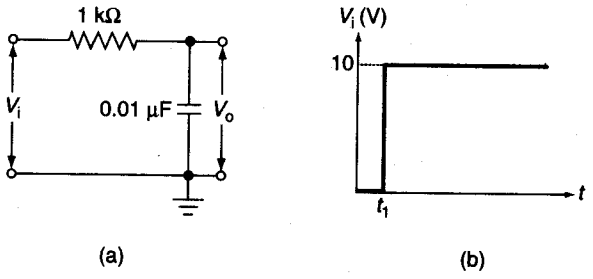



**Figure 13.6** | Example 13.2.

**Solution**

1. Circuit time constant = $RC = 10^3 \times 0.01 \times 10^{-6} = 10$ μs.
2. The response is governed by the equation

$$V_o = 10(1 - e^{-t/10^{-5}})$$
$$= 10(1 - e^{-10^5 t})$$

3. For $t = 10$ μs, $V_o = 10(1 - e^{-1}) = 0.631 \times 10 = 6.31$ V.
4. The output voltage ($V_o$) is shown in Figure 13.7.
5. The time taken for the output voltage ($V_o$) to rise from 1 V to 9 V is equal to the rise time ($t_r$):

$$t_r = 2.2RC = 2.2 \times 10^3 \times 0.01 \times 10^{-6} = 22 \text{ μs}$$

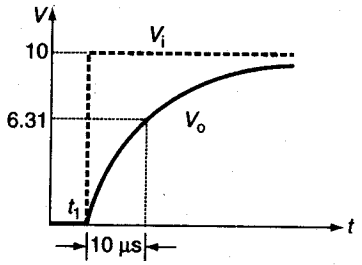



**Figure 13.7** | Solution to Example 13.2.

**EXAMPLE 13.3**

*The basic low-pass RC circuit discussed in the previous examples has 3 dB cut-off frequency of 3.5 kHz. If this circuit were fed at the input with a 20 V step, in what time will the output rise to 12.6 V starting from the time of receiving the step?*

**Solution**

1. 3 dB cut-off = 3.5 kHz.
2. Rise time = $0.35/f_{uc} = 0.35/3.5 \times 10^3 = 10^{-4}$ s.
3. Therefore, $2.2\ RC = 10^{-4}$, which gives $RC = 10^{-4}/2.2 = 45.5\ \mu s$.
4. The output will rise to 12.6 V (which is 63% of the final value of 20 V) in 45.5 μs (=time constant).

**EXAMPLE 13.4**

*Refer to Figure 13.8. Determine the output waveform ($V_o$) for 10 cycles of input waveform and comment on the results.*

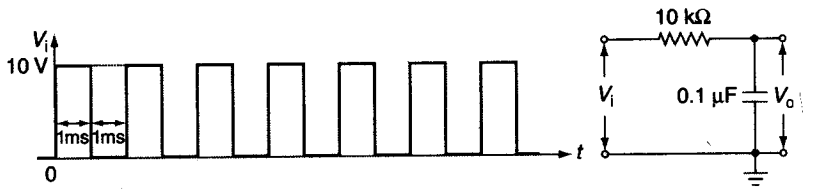



**Figure 13.8** | Example 13.4.

**Solution**

1. With the leading edge of the first cycle, the capacitor starts charging and charging is governed by the following equation, $V_o = 10(1 - e^{-t/RC})$.
2. The time constant = $RC = 10 \times 10^3 \times 0.1 \times 10^{-6} = 10^{-3}$ s = 1 ms.
3. Since the pulse high time equals the time constant (= 1 ms), the output will rise to 6.31 V at the end of the first pulse.
4. The capacitor starts discharging from the time instant of the trailing edge of the first pulse and the discharge equation is given by

$$V_o = 6.31(e^{-(t-10^{-3})/RC})$$

5. In this case, the pulse low time also equals the time constant. Therefore, at $t = 2$ ms, $V_o = 0.369 \times 6.31 = 2.33$ V.
6. With the beginning of the second pulse, the capacitor starts charging again but this time, it has an initial voltage of 2.33 V and the charging equation now would be

$$V_o = 10 - (10 - 2.33)e^{-(t-2\times10^{-3})/10^{-3}}$$

7. For, $t = 3$ ms, $V_o = 10 - 7.67 \times e^{-1} = 7.18$ V.
8. For $t = 4$ ms, $V_o = 7.18 \times 0.369 = 2.65$ V.

9. Similarly, at $t = 5$ ms,
$$V_o = 10 - (10 - 2.65) \times e^{-1} = 10 - 7.35 \times e^{-1} = 7.3 \text{ V}$$
10. At $t = 6$ ms, $V_o = 7.3 \times 0.369 = 2.69$ V.
11. At $t = 7$ ms, $V_o = 10 - (10 - 2.69) \times e^{-1} = 10 - 7.31 \times e^{-1} = 7.31$ V.
12. At $t = 8$ ms, $V_o = 7.31 \times 0.369 = 2.70$ V.
13. At $t = 9$ ms, $V_o = 10 - (10 - 2.70) \times e^{-1} = 10 - 7.30 \times e^{-1} = 7.31$ V.
14. At $t = 10$ ms, $V_o = 7.31 \times 0.369 = 2.70$ V.
15. In the subsequent cycles, the output will swing between 2.70 V and 7.31 V. It is clear from the above calculations that the steady state is achieved after four cycles. It can be verified that if the circuit time constant is much smaller than the input waveform time period, the steady state would be arrived at very quickly, most likely in the first cycle itself. If the time constant is much larger than the input waveform period, it would require comparatively larger number of cycles to reach steady state. Figure 13.9 shows the output waveform.

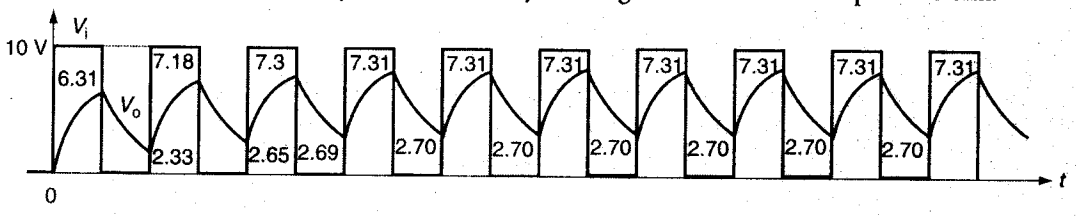



**Figure 13.9** | Solution to Example 13.4.

## 13.3 Basic RC High-Pass Circuit

Figure 13.10 shows the basic RC high-pass circuit. The operation of this circuit can be explained on lines similar to the description of RC low-pass circuit. The output voltage ($V_o$) is given by

$$V_o = \left( \frac{R}{\sqrt{R^2 + X_C{}^2}} \right) \times V_i \tag{13.12}$$

Since the reactance of a capacitor is inversely proportional to the frequency, it would increase with decrease in frequency. Consequently, the output voltage falls with decrease in frequency of the input waveform thus lending the circuit of Figure 13.10 its high-pass characteristics as shown in Figure 13.11. The frequency where the ratio $V_o/V_i$ falls to 0.707 of its maximum value is known as the lower 3 dB cut-off frequency. Expression for lower 3 dB cut-off frequency can be computed as follows:
At the lower 3 dB cut-off frequency ($f_{lc}$),

$$\frac{V_o}{V_i} = \frac{R}{\sqrt{R^2 + X_C{}^2}} = 0.707$$

Therefore at $f_{lc}$,

$$R = X_C$$

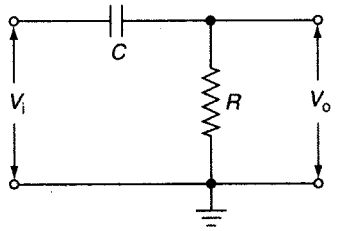



**Figure 13.10** | RC high-pass circuit.

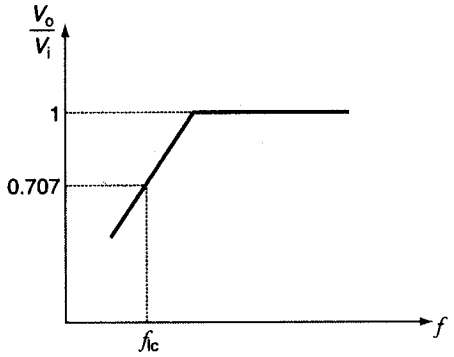



**Figure 13.11** | Frequency response of high-pass circuit.

The lower 3 dB cut-off frequency is given by

$$f_{lc} = \frac{1}{2\pi RC} \tag{13.13}$$

The lower 3 dB cut-off frequency affects the low-frequency response due to the high-pass nature of the circuit. Smaller the value of the lower 3 dB cut-off frequency, less severe is its effect on the flatter portions of the waveform. The effect of different lower 3 dB cut-off frequencies in a high-pass RC circuit for a pulsed waveform input is depicted in Figure 13.12.

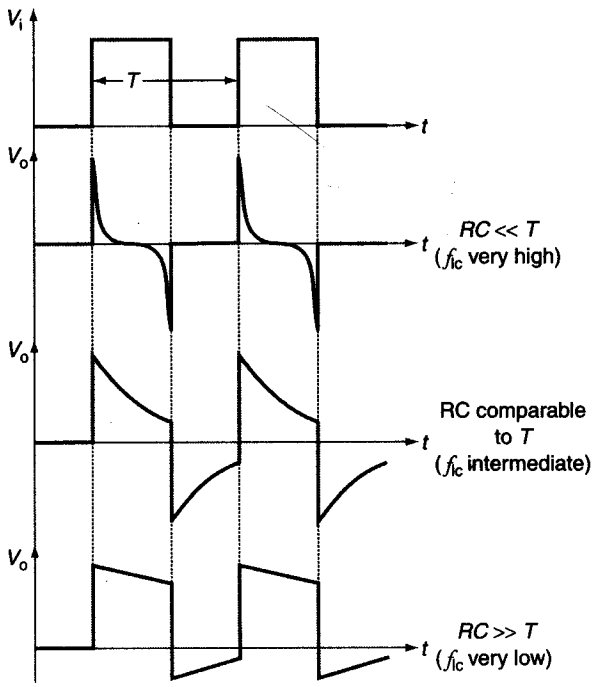



**Figure 13.12** | Effect of lower 3 dB cut-off frequency on pulsed waveform input.

## 13.4 RC High-Pass Circuit as Differentiator

A differentiator circuit is the one in which the output response is proportional to the differential of the input excitation. In other words, the output is proportional to the slope of the input. In the case of the RC circuit of Figure 13.10 where the output is taken across $R$, if the time constant ($RC$) is much smaller than the input waveform time period, it is safe to assume that whole of input ($V_i$) appears across ($C$) only as the input goes through one complete cycle. The current ($I_i$) flowing in the circuit is given by

$$I_i = C\frac{dV_i}{dt}$$

The output voltage ($V_o$) is given by

$$V_o = I_i \times R$$

$$V_o = RC\frac{dV_i}{dt} \propto \frac{dV_i}{dt} \tag{13.14}$$

This explains why RC high-pass circuit behaves as a differentiator under specified conditions.

**EXAMPLE 13.5**

*Refer to Figure 13.13. Sketch the output waveform preferably without doing any mathematical calculations.*

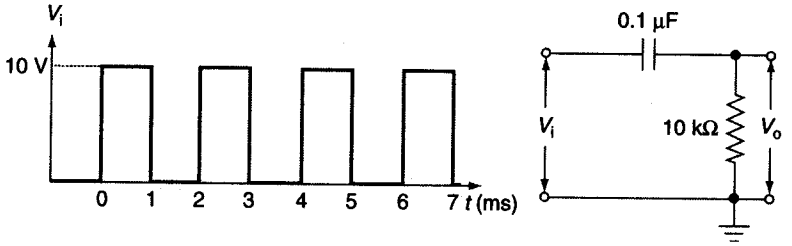



**Figure 13.13** | Example 13.5.

**Solution**

1. The output waveform is shown Figure 13.14. The waveform is self-explanatory. The fact that the circuit time constant is 1 ms and so are the high and low times of the input waveform, all voltage levels can be determined without doing any calculations.

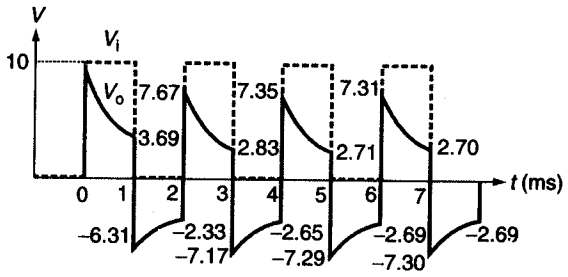



**Figure 13.14** | Solution to Example 13.5.

**EXAMPLE 13.6**

*A 100 μs pulse is applied to the RC high-pass circuit of Figure 13.15. Sketch the response waveform. Also calculate the time taken by output pulse to go to near zero after the input pulse goes low.*

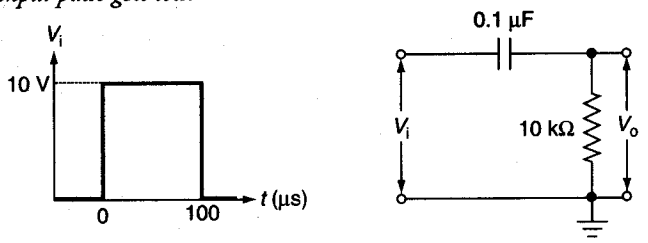



**Figure 13.15** | Example 13.6.

**Solution**

1. The output voltage at the time of termination of input pulse, that is, at $t = 100$ μs can be calculated from

$$10 - 10(1 - e^{-10^{-4}/RC}) = 10e^{-10^{-4}/10^{-3}} = 10/e^{0.1} = 9 \text{ V}$$

2. As the input pulse goes to zero, the output goes to –1 V as the voltage across capacitor cannot change instantaneously. The output then gradually rises towards zero as the capacitor discharges.
3. Since the input and output are isolated by a blocking capacitor, the output will always have a zero DC or average value. That is, area under the positive portion must equal area under the negative portion.
4. Assuming the charge and discharge process to be linear which is a valid assumption when the circuit time constant is much larger than the pulse width, we can calculate the required time for the output to decay to zero to be 1.9 ms. The response waveform is shown in Figure 13.16.

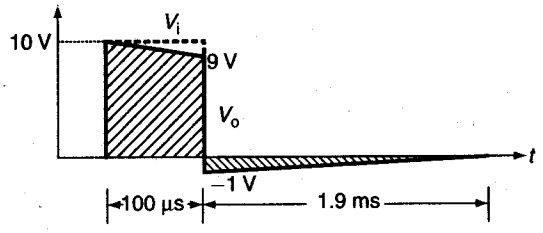



**Figure 13.16** | Solution to Example 13.6.

## 13.5 Basic RL Circuit as Integrator

Figure 13.17 shows the basic RL integrator circuit. The circuit behaves as an integrator circuit, if the time constant ($L/R$) were much larger than the time period of the input waveform. If it were so, it would be justified to assume that the current ($I_i$) is exclusively determined by $L$ as the input goes through one complete cycle. That is,

$$I_i = \frac{1}{L}\int V_i dt$$

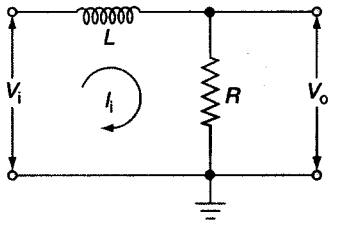



**Figure 13.17** | Basic RL integrator.

As the output voltage ($V_o$) is equal to $V_o = I_i \times R$, therefore

$$V_o = \frac{R}{L}\int V_i dt$$

$$V_o \propto \int V_i dt \tag{13.15}$$

## 13.6 Basic RL Circuit as Differentiator

Figure 13.18 shows the basic RL differentiator circuit. If the time constant ($L/R$) were much smaller than the input waveform time period, the current ($i$) very quickly reaches the steady state and the transient portion takes negligible time. It can thus be assumed that the current ($I_i$) is exclusively determined by $R$. That is,

$$I_i = \frac{V_i}{R}$$

As the output voltage ($V_o$) is equal to

$$V_o = L\frac{dI_i}{dt}$$

Therefore $V_o$ is given by

$$V_o = \frac{L}{R}\frac{dV_i}{dt}$$

$$V_o \propto \frac{dV_i}{dt} \tag{13.16}$$

We can see that the results obtained in the case of RL circuits are analogous to those obtained in the case of RC circuits. In general, for a simple integrator circuit (RL or RC),

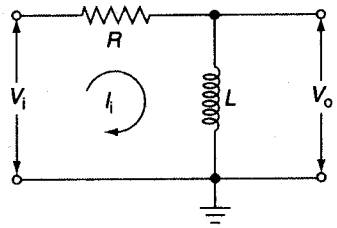



**Figure 13.18** | RL differentiator circuit.

$$V_o = \frac{1}{\tau}\int V_i dt \tag{13.17}$$

and for differentiator circuit (RL or RC)

$$V_o = \tau\left(\frac{dV_i}{dt}\right) \tag{13.18}$$

where $\tau$ is the time constant which is equal to $RC$ (for RC circuit) or $L/R$ (for RL circuit).

## 13.7 Diode Clipper Circuits

Diode-based clipper circuits can be used for clipping or removing whole or part of positive or negative portions of bidirectional waveforms. This class of wave-shaping circuits is also called non-linear wave-shaping circuits as one or more than one element has non-linear current–voltage characteristics. Four basic diode-based clipper circuits are shown in Figures 13.19(a)–(d). The non-linear element in the circuits of Figure 13.19 is the diode. In the following paragraphs, we will study the response of each of these circuits to a sinusoidal input. Diodes are assumed to be ideal. That is, the cut-in voltage of the diodes is zero.

1. The input and output waveforms for the clipping circuit of Figure 13.19(a) are shown in Figure 13.20(a). The figure is self-explanatory. The circuit configuration is similar to that of a half-wave rectifier circuit. During the positive and negative half cycles of the input waveform, the diode is respectively forward- and reverse-biased. The positive half cycles therefore appear across the output.

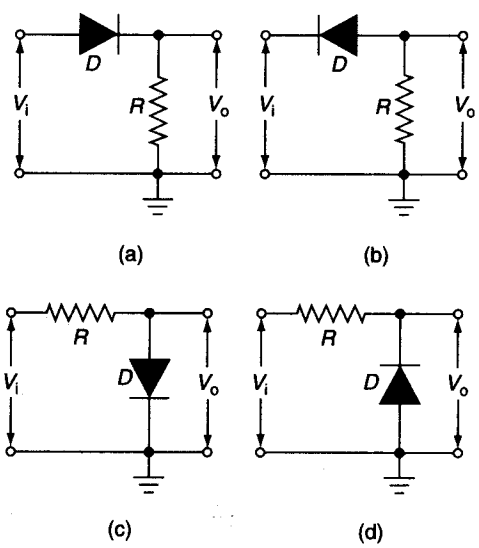



**Figure 13.19** | Basic clipper circuits.

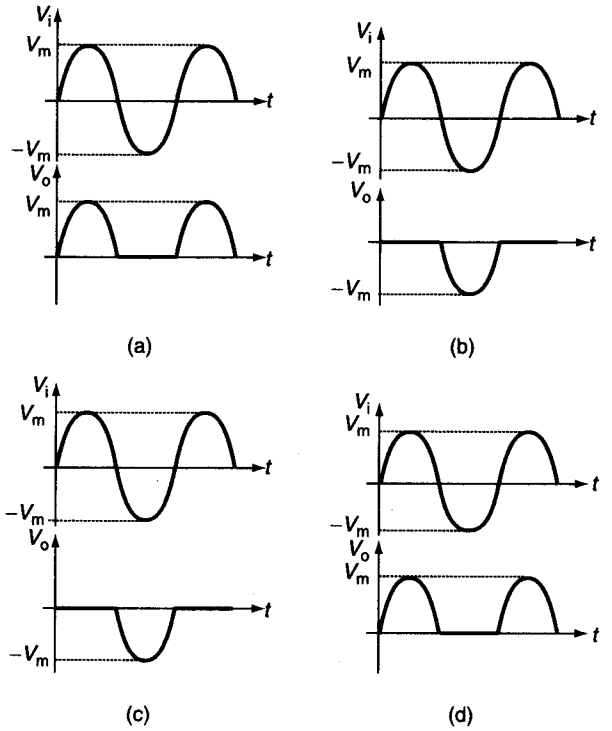



**Figure 13.20** | Input and output waveforms for the clipper circuits of Figure 13.19.

2. Similarly the output waveform for the circuit of Figure 13.19(b) is shown in Figure 13.20(b). The circuit is again a half-wave rectifier circuit that allows negative half cycles to appear across the output. The diode in this case is forward-biased during negative half cycles of the input waveform.
3. For the clipping circuit of Figure 13.19(c), the diode is forward-biased during positive half cycles and reverse-biased during negative half cycles. The output is therefore clipped to zero during positive half cycles and the negative half cycles are allowed to appear across the output as the diode is then reverse-biased.
4. For the circuit of Figure 13.19(d), the negative half cycles would be clipped to zero.

In case the diodes used in the circuits of Figure 13.19 were non-ideal, the output waveforms would be similar to those shown in Figure 13.20 except that the diode would have a cut-in voltage of 0.7 V for silicon diodes and 0.3 V for germanium diodes instead of zero as assumed in the case of ideal diodes. The waveforms for clipping circuits of Figure 13.19 with silicon diodes are shown in Figure 13.21. The other important issue is that of choice of resistance ($R$). In the case of non-ideal diodes, the forward-biased resistance of the diode ($R_f$) is not zero and also the reverse-biased resistance of the diode ($R_r$) is not infinite. In such a situation, it is desirable that resistance ($R$) is so chosen that it satisfies the condition $R_f << R << R_r$. The optimum value of $R$ is given by geometric mean of $R_f$ and $R_r$. That is

$$R = \sqrt{R_f \times R_r} \tag{13.19}$$

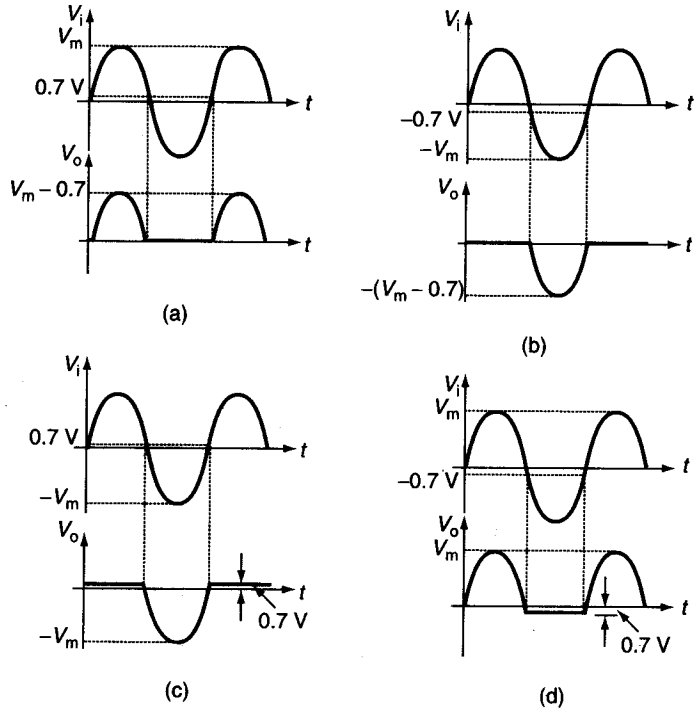



**Figure 13.21** | Output waveforms for clipper circuits of Figure 13.19 when the diodes are non-ideal.

**EXAMPLE 13.7**

*Sketch the output waveform for the clipping circuits of Figure 13.22. Assume the diodes to be ideal and the peak amplitude ($V_m$) of the input sinusoidal signal to be greater than the battery voltage ($V_{BB}$).*

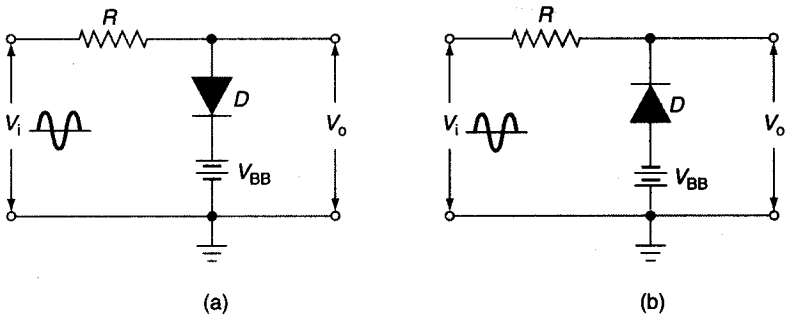



**Figure 13.22** | Example 13.7.

**Solution**

1. In the case of the circuit shown in Figure 13.22(a), the diode gets forward-biased when the input exceeds $V_{BB}$ and thus the output remains clamped at $V_{BB}$ as long as input remains greater than $V_{BB}$. For $V_i < V_{BB}$, the diode is reverse-biased and the output is same as the input. The output waveform is shown in Figure 13.23(a).
2. For the circuit of Figure 13.22(b), the diode is reverse-biased for $V_i$ less negative than $-V_{BB}$ and forward-biased for $V_i$ more negative than $-V_{BB}$. The output waveform is shown in Figure 13.23(b).

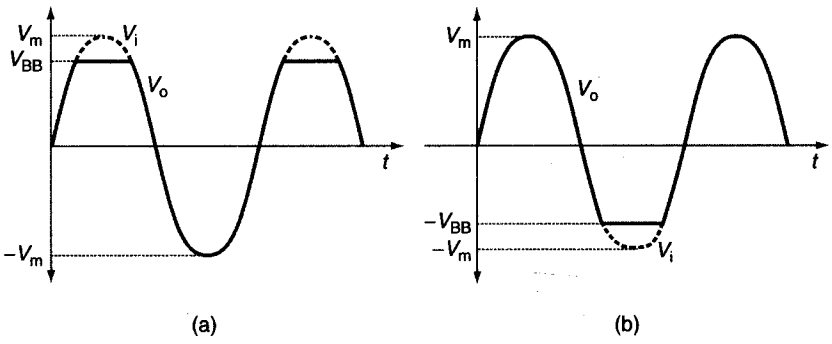



**Figure 13.23** | Solution to Example 13.7.

**EXAMPLE 13.8**

*Sketch the clipped output waveforms for the circuits of Figure 13.24. Assume the diodes to be ideal and the peak amplitude ($V_m$) of the input sinusoidal signal to be greater than battery voltage ($V_{BB}$).*

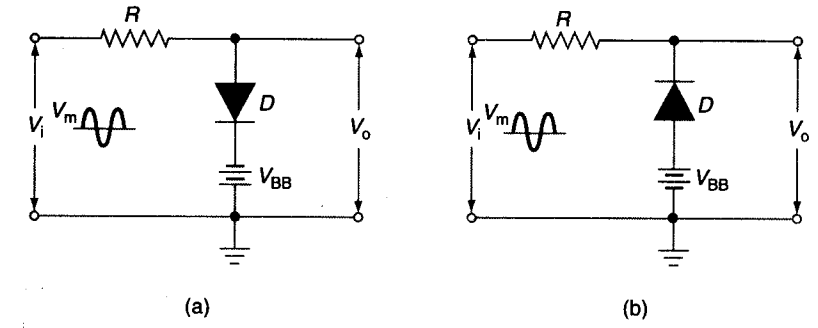



**Figure 13.24** | Example 13.8.

**Solution**

1. For the circuit shown in Figure 13.24(a), the diode is forward-biased for all input voltages except for the period when $V_i$ is more negative than the battery voltage ($-V_{BB}$) where it is reverse-biased. Figure 13.25(a) shows the output waveform.
2. For the circuit shown in Figure 13.24(b), the diode is forward-biased for $V_i$ less than equal to battery voltage ($V_{BB}$) and reverse-biased for $V_i$ greater than $V_{BB}$. Figure 13.25(b) shows the output waveform.

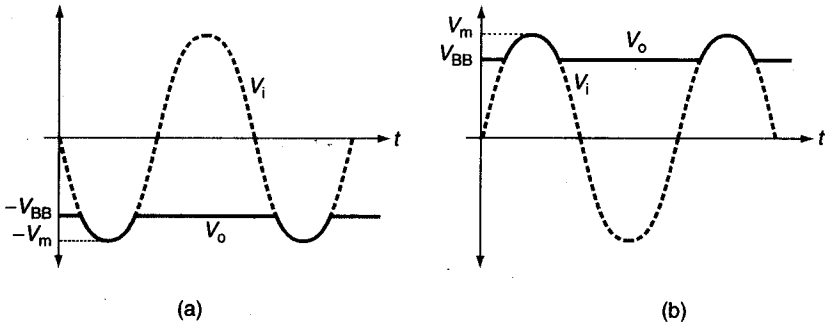



**Figure 13.25** | Solution to Example 13.8.

**EXAMPLE 13.9**

*Sketch the clipped output waveforms for the double-diode circuits of Figures 13.26(a) and (b). Assume diodes $D_1$ and $D_2$ to be ideal and the forward-biased voltage drops of the Zener diodes to be zero.*

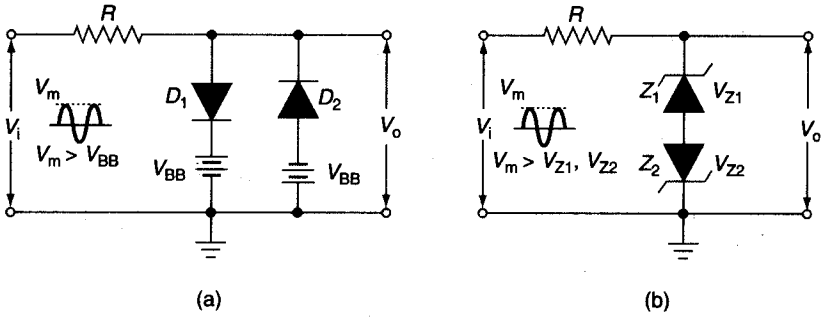



**Figure 13.26** | Example 13.9.

**Solution**

1. For the circuit shown in Figure 13.26(a), during the whole of positive half-cycle diode $D_2$ remains reverse-biased and the diode $D_1$ gets forward-biased for $V_i$ greater than $V_{BB}$.
2. During the negative half cycle, diode $D_1$ remains reverse-biased and diode $D_2$ is forward-biased only for the period where $V_i$ is more negative than $-V_{BB}$.
3. The output waveform is shown in Figure 13.27(a).
4. For the clipper circuit shown in Figure 13.26(b), Zener diode $Z_2$ is forward-biased during positive half cycle and Zener diode $Z_1$ breaks down for $V_i$ greater than $V_{Z1}$.
5. During the negative half cycle, Zener diode $Z_1$ is forward-biased and Zener diode $Z_2$ breaks down for $V_i$ more negative than $-V_{Z2}$.
6. The output waveform is shown in Figure 13.27(b).

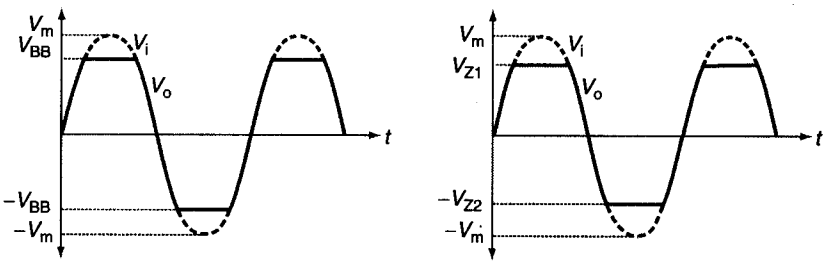



**Figure 13.27** | Solution to Example 13.9.

**EXAMPLE 13.10**

*Refer to the two diode clipper circuit of Figure 13.28(a). The input to this circuit is a linear ramp varying from 0 to 100 V as shown in Figure 13.28(b). Plot the output waveform. The diodes can be assumed to be ideal.*

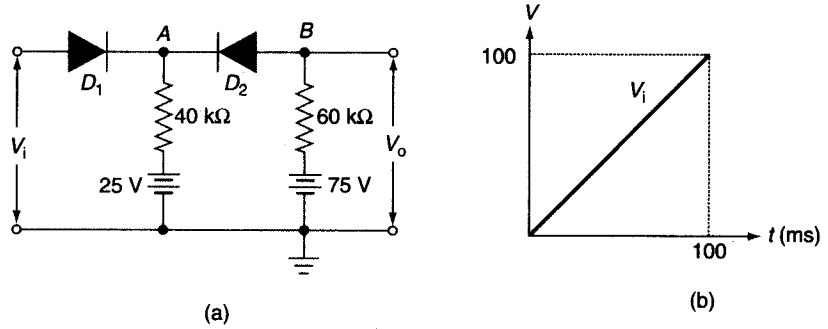



**Figure 13.28** | Example 13.10.

**Solution**

1. When the input voltage ($V_i$) is less than the potential at node $A$, the diode $D_1$ is reverse-biased.

2. When diode $D_1$ is reverse-biased and the diode $D_2$ is forward-biased, potential at node A is equal to potential at node B. The potential at nodes A and B is equal to

$$[75 - \{(75 - 25)/(60 \times 10^3 + 40 \times 10^3)\} \times 60 \times 10^3] = 45 \text{ V}$$

3. Therefore, for $V_i$ less than 45 V, diode $D_1$ is reverse-biased and diode $D_2$ is forward-biased with nodes A and B at a potential of 45 V.
4. As $V_i$ exceeds 45 V, $D_1$ gets forward-biased and from then onwards, potential at A is same as $V_i$. Diode $D_2$ remains forward-biased as long as $V_i$ does not exceed 75 V. Thus, for $V_i$ greater than 45 V and less than 75 V, $V_o$ is same as $V_i$.
5. As $V_i$ exceeds 75 V, $D_2$ is also reverse-biased. From then onwards, the output is constant at 75 V.
6. The input and output waveforms are shown in Figure 13.29.

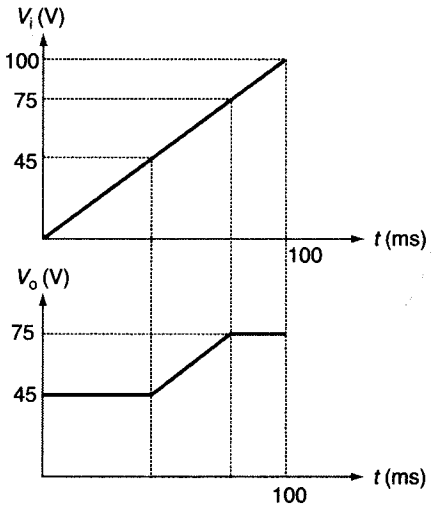



**Figure 13.29** | Solution to Example 13.10.

**EXAMPLE 13.11**

*Draw the transfer characteristics (i.e., $V_o$ versus $V_i$) for the two diode clipper circuit of Figure 13.30. Assume the diodes to be ideal.*

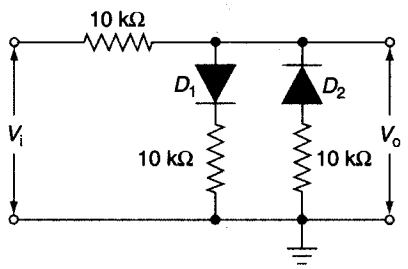



**Figure 13.30** | Example 13.11.

**Solution**

1. As $V_i$ increases in the positive direction, $D_1$ is forward-biased and $D_2$ is reverse-biased. $V_o$ in this case is always equal to $V_i/2$.
2. For negative values of $V_i$, diode $D_2$ is forward-biased and diode $D_1$ is reverse-biased. Again the output is $V_i/2$.
3. The transfer characteristics are shown in Figure 13.31.

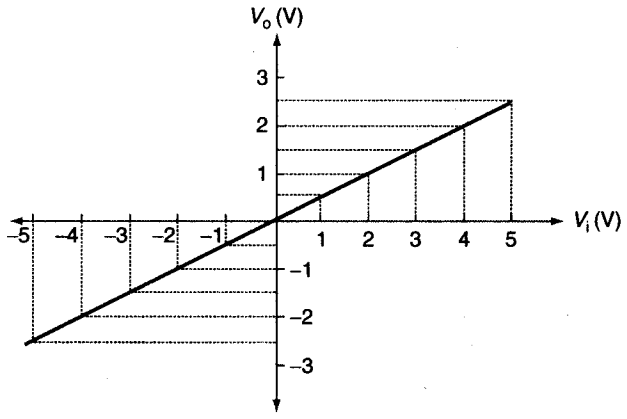



**Figure 13.31** | Solution to Example 13.11.

## 13.8 Diode Clamper Circuits

Clamper circuits are used to clamp either positive or negative extremities of an AC signal to zero. These are also called DC restorer circuits for obvious reasons. Both positive and negative clamper circuits are briefly described in the following paragraphs.

### *Negative Clamper*

Figure 13.32(a) shows the negative clamper circuit, which clamps the positive peaks of the AC signal to zero. Figure 13.32(b) shows the clamped output waveform for a given sinusoidal input. The circuit functions as follows. As the input $V_i$ rises towards the positive peak $V_m$ from zero in the first quarter of the cycle, capacitor ($C$) charges to $V_m$ through the forward-biased diode. The overall charging resistance is sum of source resistance ($R_s$), not shown in the figure, and the parallel combination of $R$ and diode's forward resistance ($R_f$). If $R$ is much larger than $R_f$ then the capacitor $C$ charges with a time constant of $[(R_s + R_f) \times C]$. Now for given $R_s$ and $R_f$, $C$ should be such that it charges to $V_m$ in a time which in no case is greater than one-fourth of the time period of the input waveform. The total charging time may be considered to be equal to five times the time constant.

When the input starts decreasing, the diode becomes reverse-biased. The capacitor now tends to discharge through resistor $R$. If the time constant ($RC$) is much larger than the time period of the input waveform, the discharge of the capacitor is negligible. Therefore, the voltage across the capacitor remains constant at the maximum value of the input signal. The output at any instant of time is then equal to algebraic sum of input voltage and voltage across the capacitor. Thus, all positive peaks ($V_m$) are clamped to zero and all

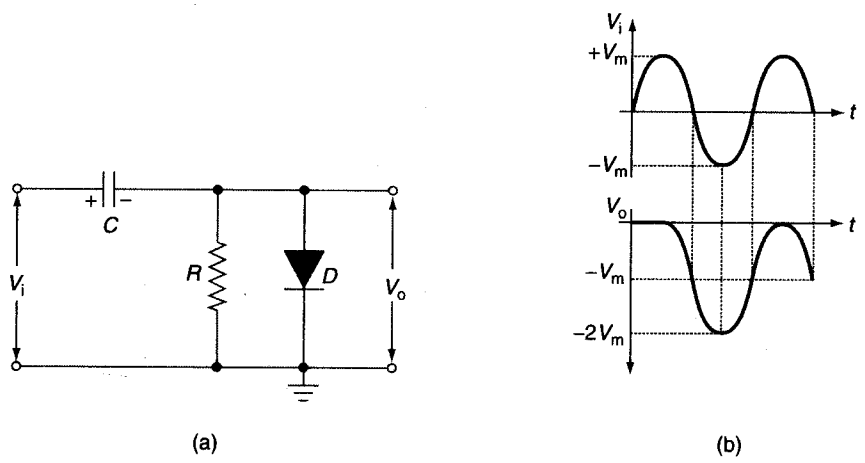



**Figure 13.32** | Negative clamper circuit.

negative peaks ($-V_m$) go to $-2V_m$. The clamping circuit as can be seen from the clamped output waveform, does not alter the wave shape, it only changes the DC level.

If the peak amplitude of the input changes, the capacitor must charge or discharge to the new value depending upon whether input amplitude has increased or decreased. When the peak value of the input signal increases, the capacitor charges through the forward-biased diode again to the new larger value and when the peak value of the input signal decreases, it discharges through $R$ to the new lower value.

In the absence of $R$, the capacitor will be forced to discharge through the reverse-biased diode resistance ($R_r$) which may be as large as 100 MΩ. Therefore, it may even be seconds before the capacitor discharges to new lower value, in case the peak amplitude of the input waveform decreases and the output again gets clamped to the desired voltage. As $R$ is chosen to be much smaller than $R_r$, this problem is not encountered and the claming is usually restored within a few cycles of the input waveform at the most even after the input undergoes a step change in peak amplitude. The optimum value of $R$ is given by geometric mean of $R_f$ and $R_r$. That is,

$$R = \sqrt{R_f \times R_r} \tag{13.20}$$

It may be mentioned here that the clamping circuit will function even in the absence of $R$ provided that the peak input amplitude remains constant. In the event of peak input amplitude decreasing, one has to wait for a sufficiently long time depending upon $R_r \times C$ time constant before normal clamping operation is restored.

After having calculated the value of $R$ for a given diode, $C$ should be so chosen that it does not discharge appreciably during the time the diode remains reverse-biased. The time constant when the diode is reverse-biased is given by

$$\left[R_s + \frac{R_r \times R}{R_r + R}\right] \times C \tag{13.21}$$

The time constant of the discharge circuit should at least be 100 times the reverse-biased time period. It is more appropriate to choose $C$ to meet extremely slow discharge requirement rather than fast charging requirement through $R_f$. $R_f$ is usually so small that $C$ chosen by the discharge criterion almost always satisfies the charge criterion.

## Positive Clamper

Figure 13.33(a) shows the positive clamper circuit. The input and output waveforms are shown in Figure 13.33(b). The circuit functions in the same way as the negative clamper circuit except that the capacitor would charge to $-V_m$ during the first negative half cycle when the diode gets forward-biased. Negative peaks are clamped to zero as for all negative peaks of the input waveform, the output ($V_o$) given by algebraic sum of $V_i$ and $V_c$ will be zero. $R$ is determined by

$$R = \sqrt{R_f \times R_r} \tag{13.22}$$

and $C$ is given by

$$\left(R_s + \frac{R_r \times R}{R_r + R}\right) \times C \geq 100\,T \tag{13.23}$$

where $T$ is the time period of the input waveform.

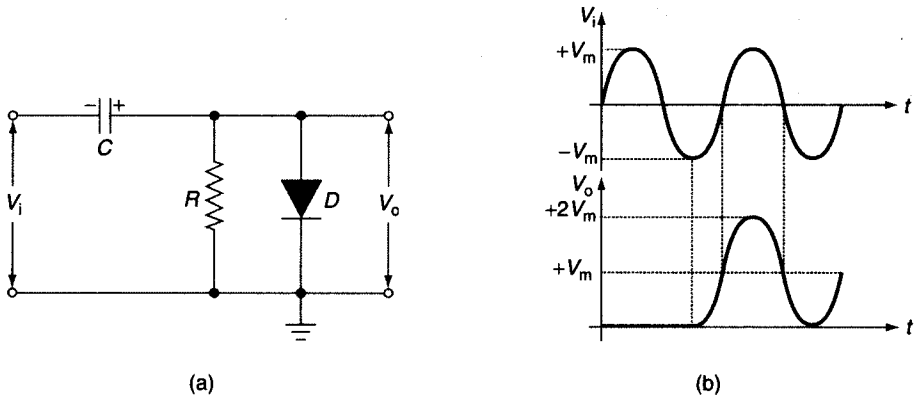



**Figure 13.33** | Positive clamper circuit.

**EXAMPLE 13.12**

*For the clamping circuit of Figure 13.34(a) and the input waveform of Figure 13.34(b), plot the output waveform for the first five cycles. Comment on the results obtained. (Assume the diodes to be ideal.)*

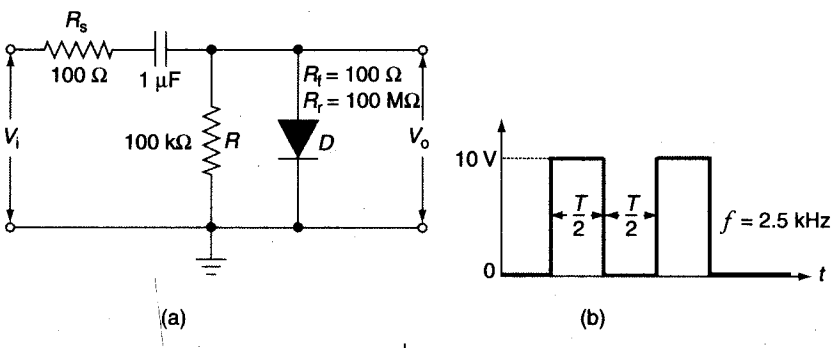



**Figure 13.34** | Example 13.12.

**Solution**

1. As the input goes from 0 to +10 V, the diode gets forward-biased. As the voltage across the capacitor cannot change instantaneously, the output voltage ($V_0$) abruptly rises to only +5 V due to the potential divider arrangement of $R_s$ (= 100 Ω) and $R_f$ (= 100 Ω).
2. The capacitor then starts charging towards +10 V with a time constant $(R_f + R_s) \times C$.
3. The time constant = $(100 + 100) \times 10^{-6} = 200$ μs.
4. The time period of input waveform = 400 μs (for $f$ = 2.5 kHz).
5. Therefore, during the first cycle, when the diode is forward-biased the capacitor would exponentially charge as per the following equation:

$$V_c = 10(1 - e^{-t/(200\times10^{-6})})$$

6. For, $t$ = 200 μs, $V_c = 10(1 - e^{-1}) = 6.3$ V.
7. This gives, $V_0 = (10 - 6.3)/2 = 1.85$ V.
8. When the input drops to zero, the diode gets reverse-biased and the output drops to –6.3 V (= capacitor voltage) as the value of $R_f$ is much larger than $R_s$.
9. For the second half of the first cycle, when the input is zero, the output remains equal to the capacitor voltage of –6.3 V. Here, it is assumed that the capacitor does not discharge through R during this time which is quite valid as the time constant ($RC$) equal to 100 ms is 500 times the half cycle time of 200 μs.
10. The output returns to +1.85 V as the input goes to +10 V again with the beginning of the second cycle. The capacitor will start charging exponentially. At the end of the HIGH time of the second cycle, the capacitor voltage $V_c = 10 - (10 - 6.3)e^{-1} = 8.64$ V.
11. This gives, $V_0 = (10 - 8.64)/2 = 0.68$ V.
12. When the input drops to zero, the output drops to –8.64 V. The output waveform progresses in the same fashion for the subsequent cycles.
13. As shown in Figure 13.35, the output is nearly clamped in the fifth cycle. From then onwards, the output has the positive extremities of the input waveform clamped to zero.

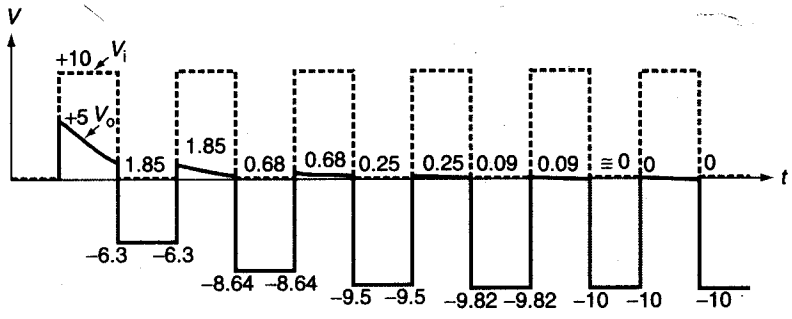



**Figure 13.35** | Solution to Example 13.12.

**EXAMPLE 13.13**

*Sketch the steady-state clamped output waveforms for the circuits shown in Figures 13.36(a)–(c). Assume a zero forward-biased voltage drop for diodes.*

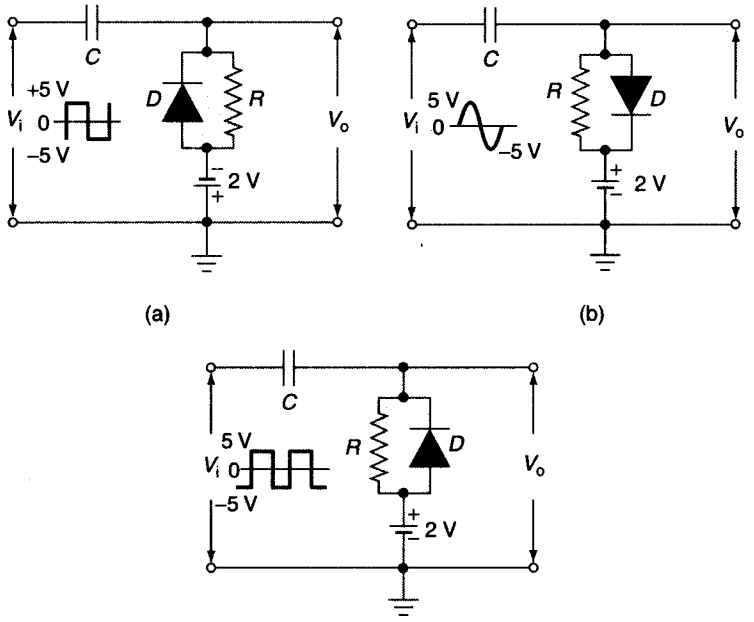



**Figure 13.36** | Example 13.13.

**Solution**

1. **Refer to Figure 13.36(a):** In the absence of the 2 V battery, the negative extremities of the input waveform would be clamped to zero. In the presence of the battery the waveform will be clamped to –2 V. Figure 13.37(a) shows the clamped waveform.
2. **Refer to Figure 13.36(b):** In this case, the positive peaks instead of being clamped to zero are clamped to +2 V. Figure 13.37(b) shows the clamped waveform.

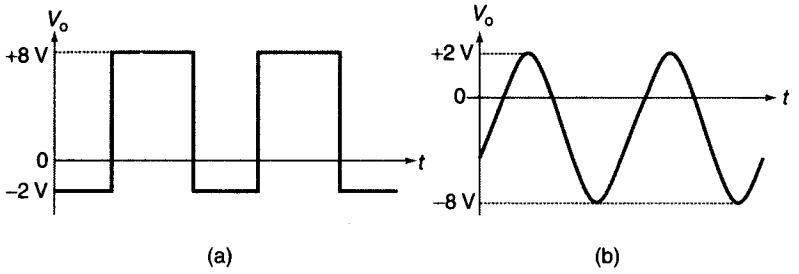
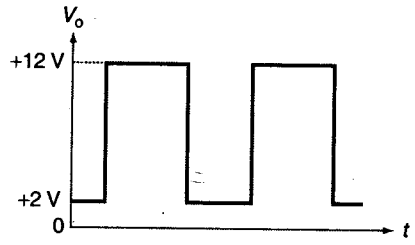



**Figure 13.37** | Solution to Example 13.13.



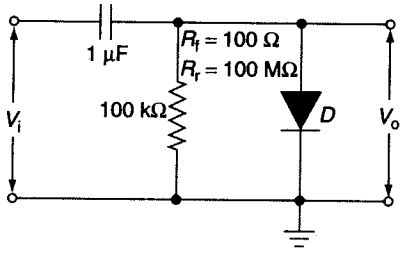

(c)

**Figure 13.37** | *Continued.*

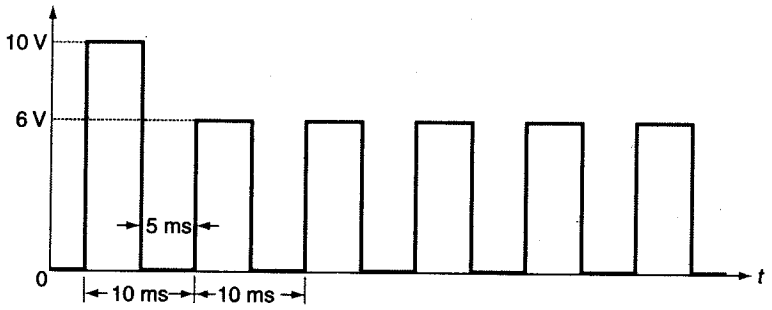
3. **Refer to Figure 13.36(c):** The circuit is similar to the one shown in Figure 13.36(a) except that the polarity of battery has been reversed. As a result, the negative peak is clamped to +2 V. Figure 13.37(c) shows the waveform.

**EXAMPLE 13.14**

*Refer to the clamping circuit of Figure 13.38(a). The input waveform to this circuit is shown in Figure 13.38(b) for the first six cycles. Sketch the clamped output waveform for the first six cycles.*




(a)




(b)

**Figure 13.38** | Example 13.14.

**Solution**

1. With $C = 1$ μF and $R_f = 100$ Ω, the capacitor ($C$) would charge to 10 V in about half a millisecond (100 μs being the charging time constant) during the 5 ms high time of the first cycle.

2. As the input drops to zero, the output too drops by 10 V and the output is at −10 V. The capacitor starts discharging the moment input goes low in the second cycle through the resistor $R$ with a time constant of 100 ms. The discharge equation is given by
$$V_c = 10e^{-(t-5\times10^{-3})/(100\times10^{-3})}$$
3. At $t = 10$ ms, the new capacitor voltage will be
$$V_c = 10e^{-(5\times10^{-3})/(100\times10^{-3})} = 10e^{-1/20} = 9.52 \text{ V}$$
4. The output voltage at $t = 10$ ms is −9.52 V.
5. With the beginning of the second cycle, the peak amplitude of the input decreases by 4 V as compared to the first cycle and as a result, the output can go up to −3.52 V and is not zero.
6. The capacitor starts discharging to 6 V with the equation
$$V_c = 6 + (9.52 - 6)e^{-(t-10\times10^{-3})/(100\times10^{-3})}$$
7. At $t = 15$ ms, the capacitor voltage will be 9.35 V and the output voltage will be −3.35 V.
8. As the input goes low, the output voltage goes to −9.35 V. The capacitor starts discharging to 0 V the moment input goes low in the second cycle with a time constant of 100 ms. The discharge equation is given by
$$V_c = 9.35e^{-(t-15\times10^{-3})/(100\times10^{-3})}$$
9. At $t = 20$ ms, the new capacitor voltage will be
$$V_c = 9.35e^{-(5\times10^{-3})/(100\times10^{-3})} = 9.35e^{-1/20} = 8.89 \text{ V}$$
The output voltage is −8.89 V.
10. With the beginning of the third cycle, the output will be −8.89 + 6 = −2.89 V.
11. With the beginning of the third cycle, the capacitor starts discharging to 6 V with the equation
$$V_c = 6 + (8.89 - 6)e^{-(t-20\times10^{-3})/(100\times10^{-3})}$$
12. At $t = 25$ ms, the capacitor voltage will be 8.75 V and the output voltage will be −2.75 V.
13. As the input goes low, the output goes to −8.75 V. The capacitor starts discharging to 0 V the moment input goes low in the third cycle with a time constant of 100 ms. The discharge equation is given by
$$V_c = 8.75e^{-(t-25\times10^{-3})/(100\times10^{-3})}$$
14. At $t = 30$ ms, the new capacitor voltage will be
$$V_c = 8.75e^{-(5\times10^{-3})/(100\times10^{-3})} = 8.75e^{-1/20} = 8.32 \text{ V}$$
15. The output voltage is −8.32 V.
16. Similar calculations can be done for the fourth, fifth and sixth cycles.
17. The output waveform is plotted in Figure 13.39.

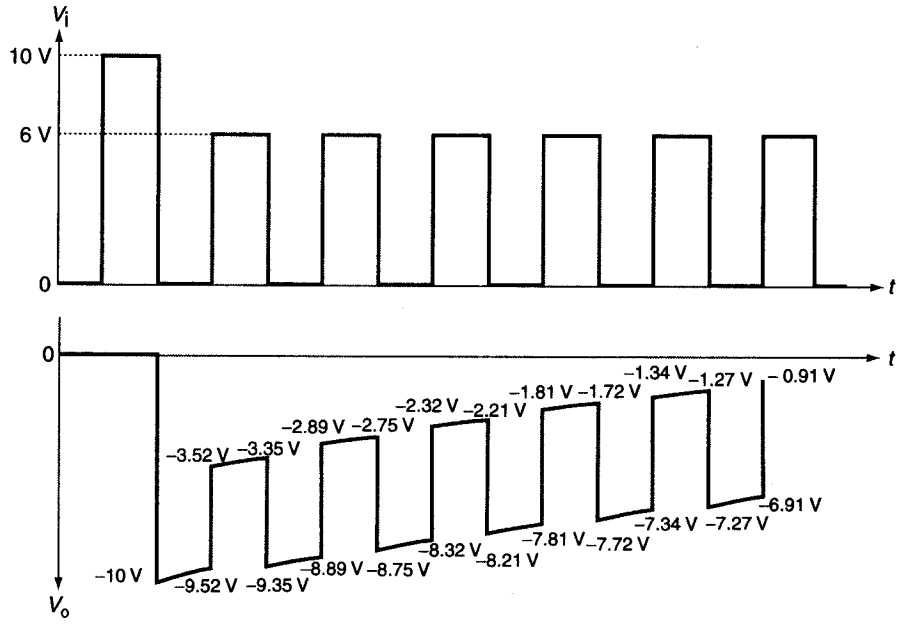



**Figure 13.39** | Solution to Example 13.14.

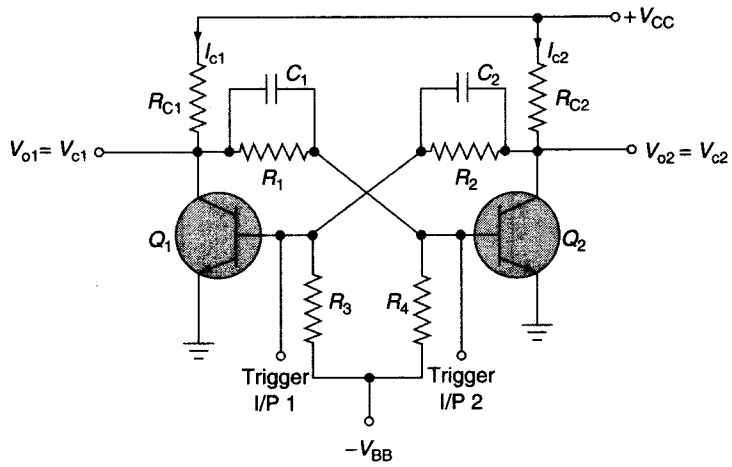
## 13.9 Multivibrators

A multivibrator like the familiar sinusoidal oscillator is a circuit with regenerative feedback with the difference that it produces a pulsed output. There are three basic types of multivibrator circuits. These include bistable multivibrator, monostable multivibrator and astable multivibrator.

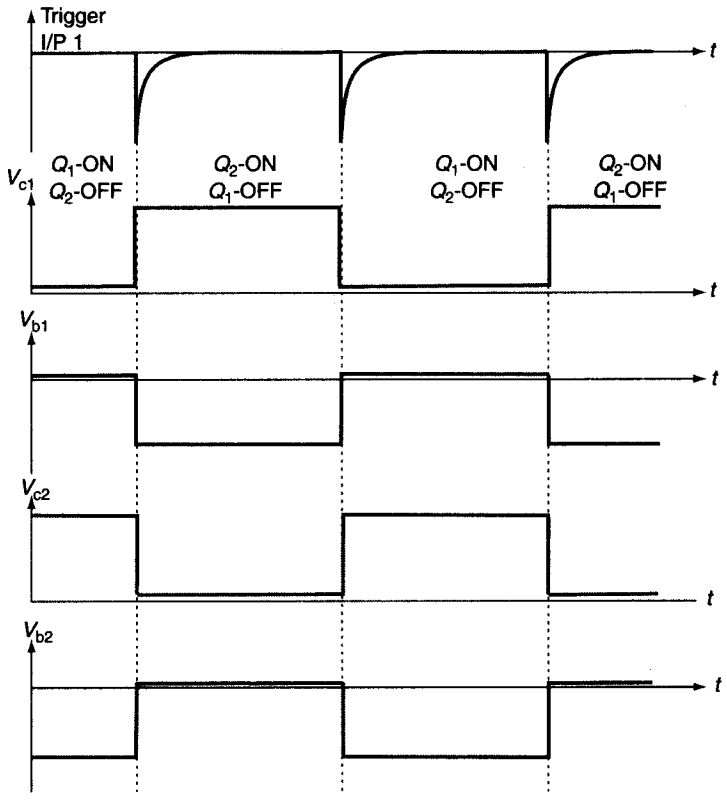
### *Bistable Multivibrator*

A *bistable multivibrator* circuit is the one in which both LOW and HIGH output states are stable. Irrespective of the logic status of the output, LOW or HIGH, it stays in that state unless a change is induced by applying an appropriate trigger pulse. As we will see subsequently, the operation of a bistable multivibrator is identical to that of a flip-flop. Figure 13.40(a) shows the basic bistable multivibrator circuit. This is the fixed-bias type of bistable multivibrator. Other configurations are self-bias type and the emitter-coupled type. However, operational principle of all types is the same. The multivibrator circuit of Figure 13.40(a) functions as follows.

In the circuit arrangement of Figure 13.40(a), it can be proved that both the transistors ($Q_1$ and $Q_2$) cannot be simultaneously ON or OFF. If $Q_1$ is ON, the regenerative feedback ensures that $Q_2$ is OFF and when $Q_1$ is OFF, the feedback drives transistor $Q_2$ to the ON-state. In order to vindicate this statement, let us assume that both the transistors $Q_1$ and $Q_2$ are conducting simultaneously. Owing to slight circuit imbalance, which is always there, collector current in one transistor will always be greater than that in the other. Let us assume that $I_{c2} > I_{c1}$. Lesser $I_{c1}$ means a higher $V_{c1}$. Since $V_{c1}$ is coupled to $Q_2$-base, rise in $V_{c1}$ leads to increase in $Q_2$-base voltage. Increase in $Q_2$-base voltage results in increase in $I_{c2}$ and associated reduction in $V_{c2}$. Reduction in $V_{c2}$ leads to reduction of $Q_1$-base voltage and an associated fall in $I_{c1}$ with the result that $V_{c1}$ increases further. Thus a slight circuit imbalance has initiated a regenerative action which culminates in transistor $Q_1$ going to cut-off




(a)




(b)

**Figure 13.40** | (a) Bistable multivibrator; (b) timing waveforms for the bistable multivibrator of (a).

and transistor $Q_2$ getting driven to saturation. To sum up, whenever there is a tendency of one of the transistors to conduct more than the other, it will end up with that transistor going to saturation and driving the other transistor to cut-off. Now, if we take output from $Q_1$ collector, it will be LOW ($=V_{CE1(sat)}$) if $Q_1$ was initially in saturation. If we apply a negative going trigger to $Q_1$-base to cause a decrease in its collector current, a regenerative action would set in which would drive $Q_2$ to saturation and $Q_1$ to cut-off. As a result, output goes to HIGH ($=+V_{CC}$) state. The output will stay HIGH till we apply another appropriate trigger to initiate a transition. Figure 13.40(b) shows the relevant timing diagrams. Thus both of the output states, when output is LOW and also when output is HIGH, are stable and undergo a change only when a transition is induced by means of an appropriate trigger pulse. That is why it is called a bistable multivibrator.

## Schmitt Trigger

Schmitt trigger circuit is a slight variation of the bistable multivibrator circuit of Figure 13.40(a). Figure 13.41 shows the basic Schmitt trigger circuit. If we compare the bistable multivibrator circuit of Figure 13.40(a) with the Schmitt trigger circuit of Figure 13.41, we find that coupling from $Q_2$-collector to $Q_1$-base in the case of bistable circuit is absent in the case of Schmitt trigger circuit. Instead, resistor $R_E$ provides the coupling. The circuit functions as follows.

When $V_{in}$ is zero, transistor $Q_1$ is in cut-off. Coupling from $Q_1$-collector to $Q_2$-base drives transistor $Q_2$ to saturation with the result that $V_o$ is LOW. If we assume that $V_{CE2\ (sat)}$ is zero, then voltage across $R_E$ is given by

$$\text{Voltage across } R_E = \frac{V_{CC} \times R_E}{R_E + R_{C2}} \tag{13.24}$$

This is also the emitter voltage of transistor $Q_1$. In order to make transistor $Q_1$ conduct, $V_{in}$ must at least be equal to 0.7 V more than the voltage across $R_E$. That is,

$$V_{in} = \frac{V_{CC} \times R_E}{R_E + R_{C2}} + 0.7 \tag{13.25}$$

When $V_{in}$ exceeds this voltage, $Q_1$ starts conducting. The regenerative action again drives $Q_2$ to cut-off. The output goes to the HIGH state. Voltage across $R_E$ changes to a new value given by

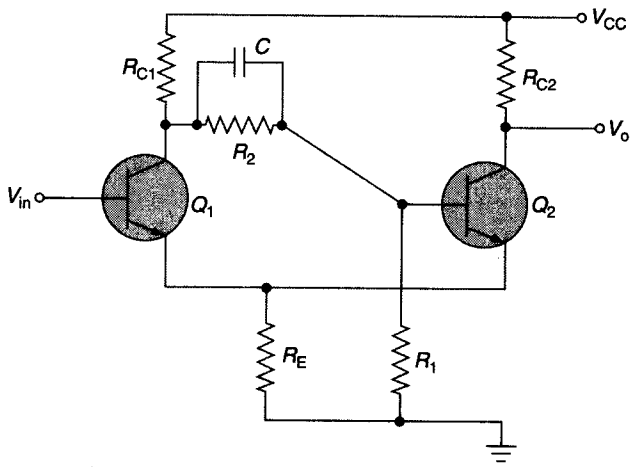



**Figure 13.41** | Schmitt trigger.

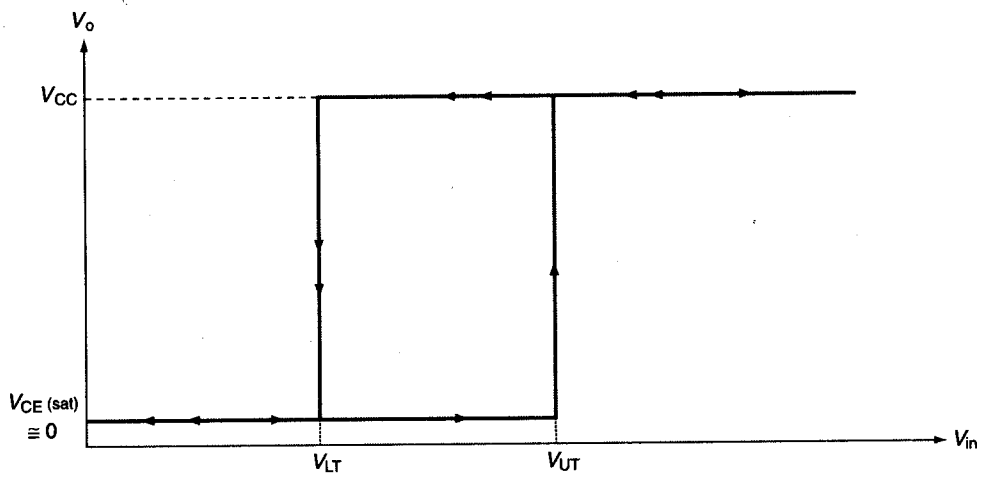



**Figure 13.42** | Transfer characteristics of the Schmitt trigger circuit.

$$\text{Voltage across } R_E = \frac{V_{CC} \times R_E}{R_E + R_{C1}} \tag{13.26}$$

$Q_1$ will continue to conduct as long as $V_{in}$ is equal to or greater than the value given by

$$V_{in} = \frac{V_{CC} \times R_E}{R_E + R_{C1}} + 0.7 \tag{13.27}$$

If $V_{in}$ falls below this value, $Q_1$ tends to come out of saturation and conduct less heavily. The regenerative action does the rest with the process culminating in $Q_1$ going to cut-off and $Q_2$ to saturation. Thus the state of output (HIGH or LOW) depends upon input voltage level. The HIGH and LOW states of the output correspond to two distinct input levels given by Eqs. (13.25) and (13.27) and therefore they depend on the values of $R_{C1}$, $R_{C2}$, $R_E$ and $V_{CC}$. Schmitt trigger circuit of Figure 13.41 therefore exhibits hysteresis. Figure 13.42 shows the transfer characteristics of the Schmitt trigger circuit. The lower trip point ($V_{LT}$) and upper trip point ($V_{UT}$) of these characteristics are, respectively, given by Eqs. (13.28) and (13.29):

$$V_{LT} = \frac{V_{CC} \times R_E}{R_E + R_{C1}} + 0.7 \tag{13.28}$$

$$V_{UT} = \frac{V_{CC} \times R_E}{R_E + R_{C2}} + 0.7 \tag{13.29}$$

## Monostable Multivibrator

A *monostable multivibrator*, also known as *monoshot*, is the one in which one of the states is stable and the other is quasi-stable. The circuit is initially in the stable state. It goes to the quasi-stable state when appropriately triggered. It stays in the quasi-stable state for a certain time period, after which it comes back to the stable state. Figure 13.43 shows the basic monostable multivibrator circuit. The circuit functions as follows. Initially, transistor $Q_2$ is in saturation as it gets its base bias from $+V_{CC}$ through $R$. Coupling from $Q_2$-collector to $Q_1$-base ensures that $Q_1$ is in cut-off. When a positive trigger pulse of short duration and sufficient magnitude is applied

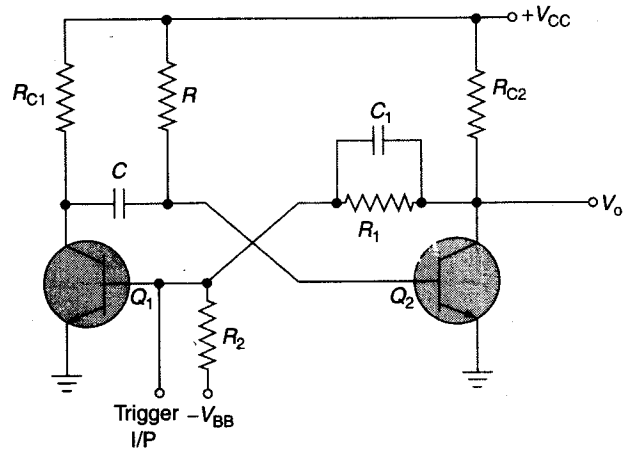



**Figure 13.43** | Monostable multivibrator.

to the base of transistor $Q_1$, $Q_1$ starts conducting. As the voltage across the capacitor $C$ cannot change instantly, negative voltage is applied to the base of transistor $Q_2$ and it turns OFF. Therefore, the output goes to the HIGH state. In other words, since there is no direct coupling from $Q_1$-collector to $Q_2$-base, which is necessary for a regenerative process to set in, $Q_1$ is not necessarily in saturation. However, it conducts some current. The $Q_1$-collector voltage falls by $I_{c1}R_{C1}$ and $Q_2$-base voltage falls by the same amount as voltage across a capacitor ($C$ in this case) can not change instantaneously. To sum up, the moment we applied the trigger, $Q_2$ went to cut-off and $Q_1$ started conducting. But now there is a path for capacitor $C$ to charge from $V_{CC}$ through $R$ and the conducting transistor. The polarity of voltage across $C$ is such that $Q_2$-base potential rises. The moment $Q_2$-base voltage exceeds the cut-in voltage, it turns $Q_2$ ON, which due to coupling through $R_1$ turns $Q_1$ OFF. And we are back to the original state, the stable state. Figure 13.44 shows the relevant timing diagrams. Whenever, we trigger the circuit into the other state, it does not stay there permanently and returns back after a time period that depends upon $R$ and $C$. Larger the time constant ($RC$), larger is the time for which it stays in the other state called quasi-stable state. The width of the quasi-stable state is given by

$$T = 0.693 \times R \times C \tag{13.30}$$

### *Retriggerable Monostable Multivibrator*

In a conventional monostable multivibrator, once the output is triggered to the quasi-stable state by applying a suitable trigger pulse, the circuit does not respond to subsequent trigger pulses as long as the output is in quasi-stable stable. After the output returns to its original state, it is ready to respond to the next trigger pulse. There is another class of monostable multivibrators called *retriggerable monostable multivibrators*, which responds to trigger pulses even when the output is in quasi-stable state. In this class of monostable multivibrators, if $n$ trigger pulses with a time period of $T_t$ are applied to the circuit, the output pulse width, that is, the time period of the quasi-stable state equals $(n-1)T_t + T$, where $T$ is the output pulse width for the single trigger pulse and $T_t < T$. Figure 13.45 shows output pulse width in the case of a retriggerable monostable multivibrator for repetitive trigger pulses.

## Astable Multivibrator

In the case of an astable multivibrator, neither of the two states is stable. Both output states are quasi-stable. The output switches from one state to the other and the circuit functions like a free-running square wave

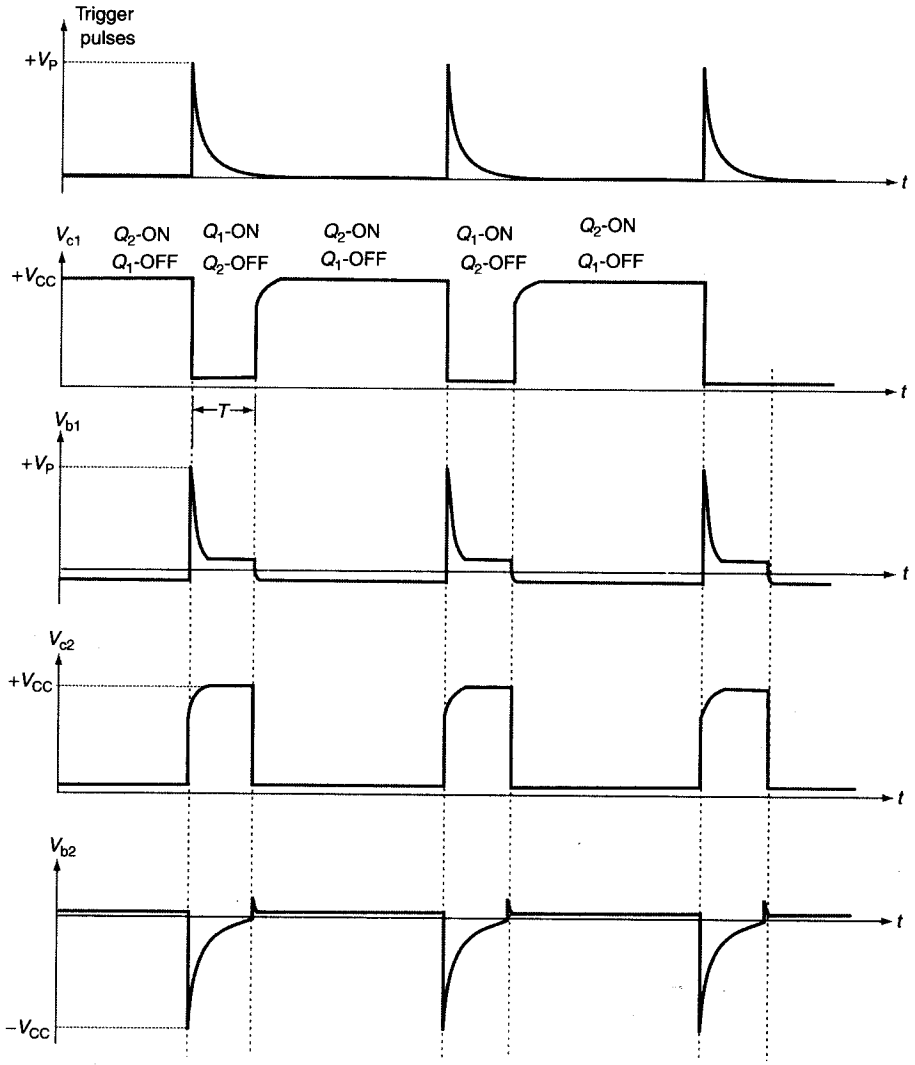



**Figure 13.44** | Timing waveforms of monostable multivibrator.

oscillator. Figure 13.46 shows the basic astable multivibrator circuit. Value of resistors $R_1$ and $R_2$ are typically 10 times the values of $R_{C1}$ and $R_{C2}$, respectively. It can be proved that in this type of circuit, neither of the output states is stable. Both states, LOW as well as HIGH, are quasi-stable. The time periods for which the output remains LOW and HIGH depends upon $R_2C_2$ and $R_1C_1$ time constants, respectively. For $R_1C_1 = R_2C_2$, the output is a symmetrical square waveform. The circuit functions as follows. When power is applied, one transistor will conduct more than the other because of some circuit imbalances. Let us assume that transistor $Q_1$ conducts more than transistor $Q_2$. The regenerative action will force transistor $Q_1$ to saturation and transistor $Q_2$ to cut-off. Capacitor $C_2$ will charge rapidly to $V_{CC}$ through resistor $R_{C2}$ and the emitter–base junction of transistor $Q_1$. This results in momentary increase in the base voltage of transistor $Q_1$. Capacitor $C_1$

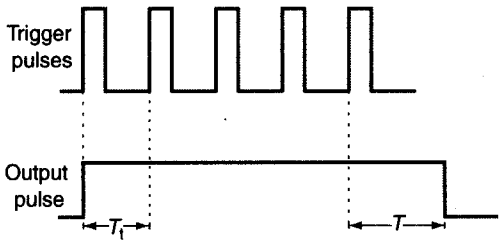



**Figure 13.45** Output pulse width for retriggerable monostable multivibrator for repetitive trigger pulses.

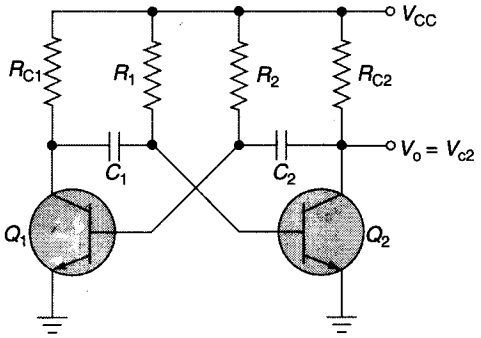



**Figure 13.46** Astable multivibrator.

had previously charged through resistor $R_{C1}$ upto $V_{CC}$ when transistor $Q_2$ was conducting. Now when $Q_1$ is conducting, $C_1$ discharges through $R_1$ and $Q_1$. The initial pulse of discharge current from $C_1$ through $R_1$ results in a negative pulse at the base of transistor $Q_2$ as shown in Figure 13.47. This turns transistor $Q_2$ OFF and the output goes to HIGH state. Transistor $Q_1$ keeps conducting from $V_{CC}$ through resistor $R_2$. The OFF-time of transistor $Q_2$ depends upon the time constant $R_1C_1$. When the base voltage of the transistor reaches the base-switching voltage, transistor $Q_2$ is no longer in cut-off and starts to conduct allowing capacitor $C_1$ to be recharged rapidly through resistor $R_{C1}$. This results in momentary increase in positive voltage at the base of the transistor $Q_2$ leading to its fast turning ON. Therefore, the output goes to the LOW state. Now capacitor $C_2$ discharges through transistor $Q_2$ and resistor $R_2$. The initial pulse of discharge current from $C_2$ through $R_2$ makes the base of transistor $Q_1$ very negative. This turns OFF $Q_1$. $Q_1$ is held in the OFF-state depending upon the time constant $R_2C_2$ after which $Q_1$ begins to conduct. This process continues and due to both the couplings ($Q_1$-collector to $Q_2$-base and $Q_2$-collector to $Q_1$-base) being capacitive, neither of the states is stable. The rounding off in the rising edge of $V_{c1}$ is because of the voltage drop across resistor $R_{C1}$ while capacitor $C_1$ is recharging. Similarly the rounding off in the rising edge of $V_{c2}$ is because of the voltage drop across resistor $R_{C2}$ while capacitor $C_2$ is recharging. Figure 13.47 shows the relevant timing diagrams.

Let us now determine the frequency of the output wave for the astable multivibrator of Figure 13.46. The base voltage of transistor $Q_2$ during discharge of capacitor $C_1$ is given by

$$V_{b2} = V_{CC} - I_{c1}R_1 \tag{13.31}$$

Since, the capacitor charges to approximately $V_{CC}$, the initial value of current ($I_{c1}$) is

$$I_{c1} = \frac{V_{CC} + V_{CC}}{R_1} = \frac{2V_{CC}}{R_1}$$

The current decays exponentially with a time constant of $R_1C_1$. Therefore, the voltage $V_{b2}$ is given by

$$V_{b2} = V_{CC} - 2V_{CC}e^{-t/R_1C_1} \tag{13.32}$$

The base-switching voltage for silicon transistors is 0.7 V and that for germanium transistors is 0.3 V, which is very small as compared to the $V_{CC}$ voltage. Therefore, it can be assumed that the transistor will switch when $V_{b2} = 0$ V. The time required to switch ON transistor $Q_2$, that is, the OFF time of the transistor $Q_2$ ($T_2$) is given by

$$0 = V_{CC} - 2V_{CC}e^{-T_2/R_1C_1}$$

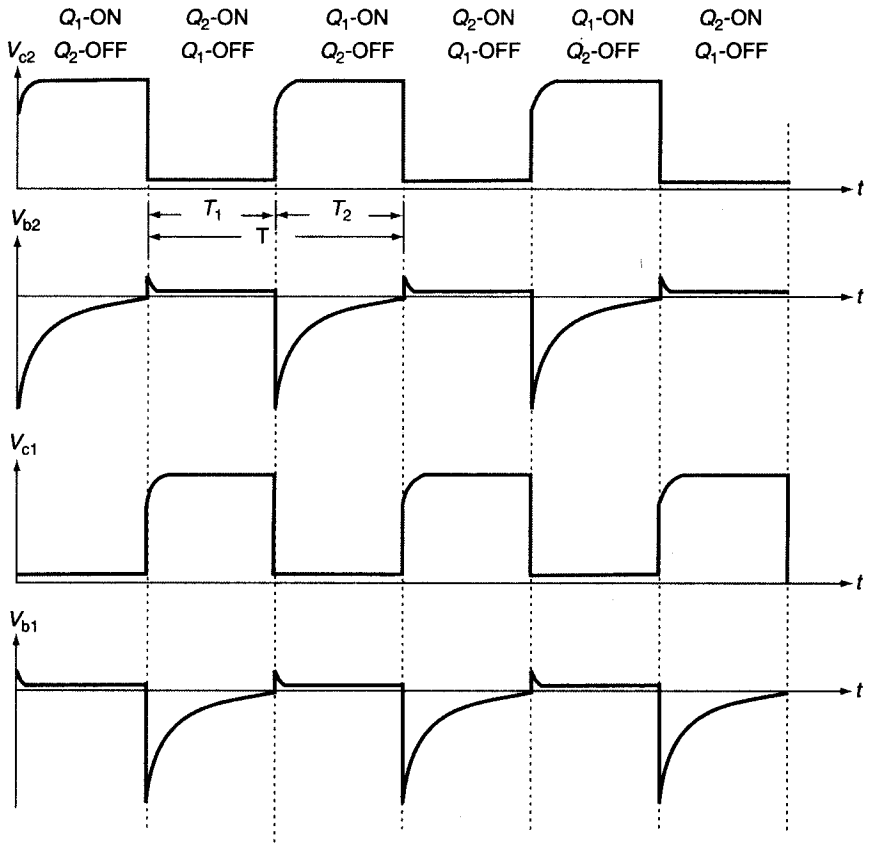



**Figure 13.47** Timing waveforms of astable multivibrator.

Therefore,

$$T_2 = R_1C_1 \ln 2 = 0.694R_1C_1 \tag{13.33}$$

$T_2$ is also the ON time of transistor $Q_1$. Similarly, the ON time of transistor $Q_2$ ($T_1$) which is equal to the OFF time of transistor $Q_1$ is given by

$$T_1 = R_2C_2 \ln 2 = 0.694R_2C_2 \tag{13.34}$$

The total time period of the wave is $T$ which is given by

$$T = T_1 + T_2 = 0.694(R_1C_1 + R_2C_2) \tag{13.35}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the time period is given by $T = 1.388RC$ and the frequency ($f$) is given by

$$f = \frac{1}{1.388RC}$$

## 13.10 Integrated Circuit (IC) Multivibrators

In this section, we will discuss monostable and astable multivibrator circuits that can be configured around some of the popular digital and linear integrated circuits.

### *Digital IC-Based Monostable Multivibrators*

Some of the commonly used digital ICs that can be used as monostable multivibrators include 74121 (single monostable multivibrator), 74221 (dual monostable multivibrator), 74122 (single retriggerable monostable multivibrator), 74123 (dual retriggerable monostable multivibrator) – all belonging to TTL family and 4098B (dual retriggerable monostable multivibrator) belonging to CMOS family. Figure 13.48 shows the use of IC 74121 as a monostable multivibrator along with trigger input. The IC provides features for triggering on either LOW-to-HIGH or HIGH-to-LOW edges of the trigger pulses. Figure 13.48(a) shows one of possible application circuits for HIGH-to-LOW edge triggering and Figure 13.48(b) shows one of possible application circuits for LOW-to-HIGH edge triggering. Output pulse width depends on external $R$ and $C$. The output pulse width can be computed from $T = 0.7RC$. Recommended ranges of values for $R$ and $C$, respectively, are 4 kΩ to 40 kΩ and 10 pF to 1000 μF. 74121 IC provides complementary outputs. That is, we have stable LOW or HIGH state and corresponding quasi-stable HIGH or LOW state available on $Q$ and $\overline{Q}$ outputs.

Figure 13.49 shows the use of 74123, a dual retriggerable monostable multivibrator. Like 74121, this IC too provides features for triggering on either LOW-to-HIGH or HIGH-to-LOW edges of the trigger pulses. Output pulse width depends on external $R$ and $C$. It can be computed from $T = 0.28RC \times [1 + (0.7/RC)]$, where $R$ and $C$ are, respectively, in kilo-ohms and pico-farads and $T$ is in nano-seconds. This formula is valid for $C > 1000$ pF. Recommended range of values for $R$ is 5–50 kΩ. Figures 13.49(a) and (b) give application circuits for HIGH-to-LOW and LOW-to-HIGH triggering, respectively. It may be mentioned here that, there can be other triggering circuit options for both HIGH-to-LOW and LOW-to-HIGH edge triggering of the monostable mulitvibrator.

### *Timer IC-Based Multivibrators*

Timer IC 555 is one of the most commonly used general-purpose linear integrated circuits. The simplicity with which monostable and astable multivibrator circuits can be configured around this IC is one of the main reasons for its wide use. Figure 13.50 shows the internal schematic of timer IC 555. It comprises two

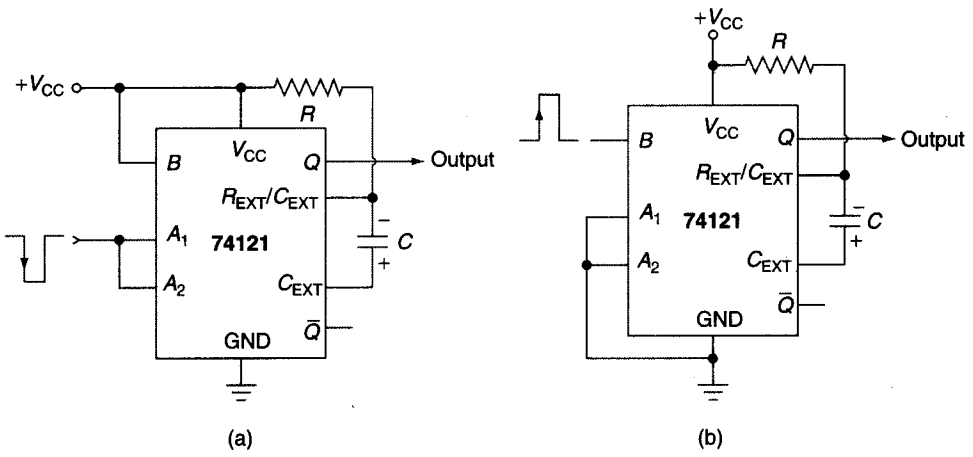



**Figure 13.48** | (a) HIGH-to-LOW edge triggering of 74121; (b) LOW-to-HIGH edge triggering of 74121.

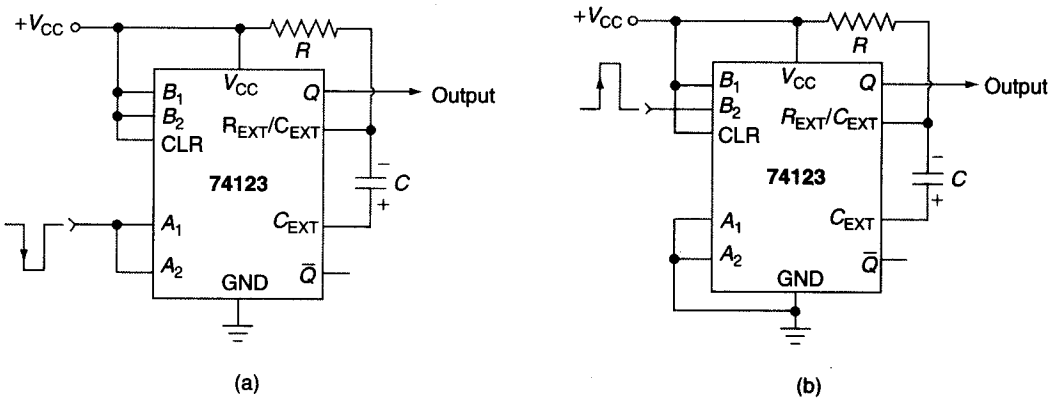



**Figure 13.49** | (a) HIGH-to-LOW edge triggering of 74123; (b) LOW-to-HIGH edge triggering of 74123.

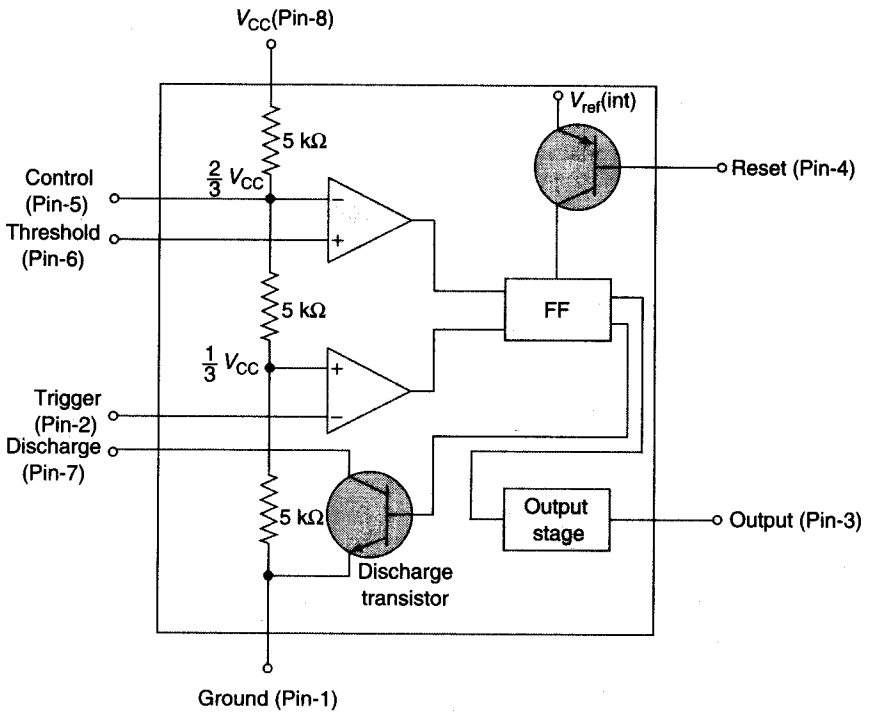



**Figure 13.50** | Internal schematic of timer IC 555.

opamp comparators, a flip-flop, a discharge transistor, a reset transistor, three identical resistors and an output stage. The resistors set the reference voltage levels at the non-inverting input of the lower comparator and inverting inputs of the upper comparator at $+V_{CC}/3$ and $+2V_{CC}/3$, respectively. Outputs of two comparators feed SET and RESET inputs of the flip-flop and thus decide the logic status of its output and subsequently the final output. The flip-flop's complementary outputs feed the output stage and the base of the

discharge transistor. This ensures that when the output is HIGH, the discharge transistor is OFF and when the output is LOW, the discharge transistor is ON. Different terminals of the timer 555 are designated as *Ground* (Terminal-1), *Trigger* (Terminal-2), *Output* (Terminal-3), *Reset* (Terminal-4), *Control* (Terminal-5), *Threshold* (Terminal-6), *Discharge* (Terminal-7) and $+V_{CC}$ (Terminal-8). With this background, we will now describe the astable and monostable multivibator circuits configured around timer IC 555.

### *Astable Multivibrator Using Timer IC 555*

Figure 13.51(a) shows the basic 555 timer-based astable multivibrator circuit. Initially, capacitor $C$ is fully discharged, which forces output to go to the HIGH-state. An open discharge transistor allows capacitor $C$ to charge from $+V_{CC}$ through $R_1$ and $R_2$. When the voltage across $C$ exceeds $+2V_{CC}/3$, the output goes to the LOW-state and the discharge transistor is switched ON at the same time. Capacitor $C$ begins to discharge through $R_2$ and the discharge transistor inside the IC. When the voltage across $C$ falls below $+V_{CC}/3$, the output goes back to the HIGH-state. The charge and discharge cycles repeat and the circuit behaves like a free-running multivibrator. Terminal-4 of the IC is the RESET terminal. Usually, it is connected to $+V_{CC}$. If the voltage at this terminal is driven below 0.4 V, the output is forced to the LOW-state overriding command pulses at Terminal-2 of the IC. HIGH-state and LOW-state time periods are governed by the charge ($+V_{CC}/3$ to $+2V_{CC}/3$) and discharge ($+2V_{CC}/3$ to $+V_{CC}/3$) timings. These are given by Eqs. (13.36) and (13.37), respectively.

$$\text{HIGH-state time period, } T_{HIGH} = 0.69 \times (R_1 + R_2) \times C \tag{13.36}$$

$$\text{LOW-state time period, } T_{LOW} = 0.69 \times R_2 \times C \tag{13.37}$$

The relevant waveforms are shown in Figure 13.51(b). The time period ($T$) and frequency ($f$) of the output waveform are, respectively, given by Eqs. (13.38) and (13.39), respectively.

$$\text{Time period, } T = 0.69 \times (R_1 + 2R_2) \times C \tag{13.38}$$

$$\text{Frequency, } f = \frac{1}{0.69 \times (R_1 + 2R_2) \times C} \tag{13.39}$$

Remember that when the astable multivibrator is powered, first cycle HIGH-state time period is about 30% longer as the capacitor is initially discharged and it charges from 0 (rather than $+V_{CC}/3$) to $+2V_{CC}/3$.

In the case of the astable multivibrator circuit of Figure 13.51(a), the HIGH-state time period is always greater than the LOW-state time period. Figures 13.51(c) and (d) show two modified circuits where HIGH-state and LOW-state time periods can be chosen independently. For the astable multivibrator circuits of Figures 13.51(c) and (d), the two time periods are given by Eqs. (13.40) and (13.41), respectively.

$$\text{HIGH-state time period} = 0.69 \times R_1 \times C \tag{13.40}$$

$$\text{LOW-state time period} = 0.69 \times R_2 \times C \tag{13.41}$$

For $R_1 = R_2 = R$

$$T = 1.38 \times R \times C$$

$$f = \frac{1}{1.38 \times R \times C} \tag{13.42}$$

### *Monostable Multivibrator Using Timer IC 555*

Figure 13.52(a) shows the basic monostable multivibrator circuit configured around timer 555. It may be mentioned here that monostable multivibrators are also referred to as monoshots. Trigger pulse is applied to Terminal-2

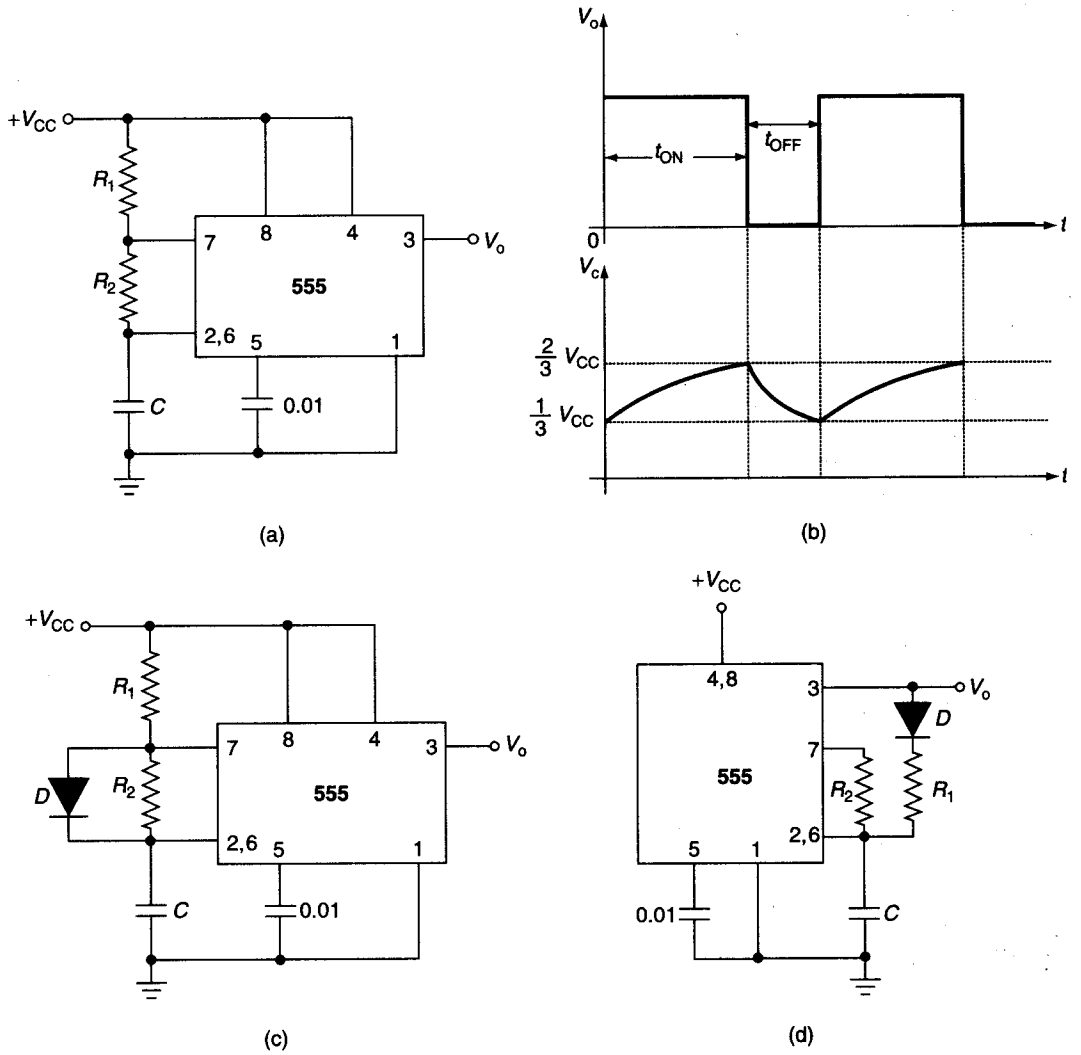



**Figure 13.51** (a) Astable multivibrator; (b) relevant waveforms for (a); (c) and (d) modified astable multivibrator circuits.

of the IC, which should initially be kept at $+V_{CC}$. A HIGH at Terminal-2 forces the output to LOW-state. A HIGH-to-LOW trigger pulse at Terminal-2 holds the output in the HIGH-state and simultaneously allows the capacitor to charge from $+V_{CC}$ through $R$. Remember that LOW-level of the trigger pulse needs to go at least below $+V_{CC}/3$. When the capacitor voltage exceeds $+2V_{CC}/3$, the output goes back to the LOW-state. We will need to apply another trigger pulse to Terminal-2 to make the output go to the HIGH-state again. Every time the timer is appropriately triggered, the output goes to the HIGH-state and stays there for a time period taken by capacitor to charge from 0 to $+2V_{CC}/3$. This time period, which equals the monoshot output pulse width, is given by

$$T = 1.1 \times R \times C \tag{13.43}$$

Figure 13.52(b) shows relevant wacefroms for the circuit of figure 13.52(a).

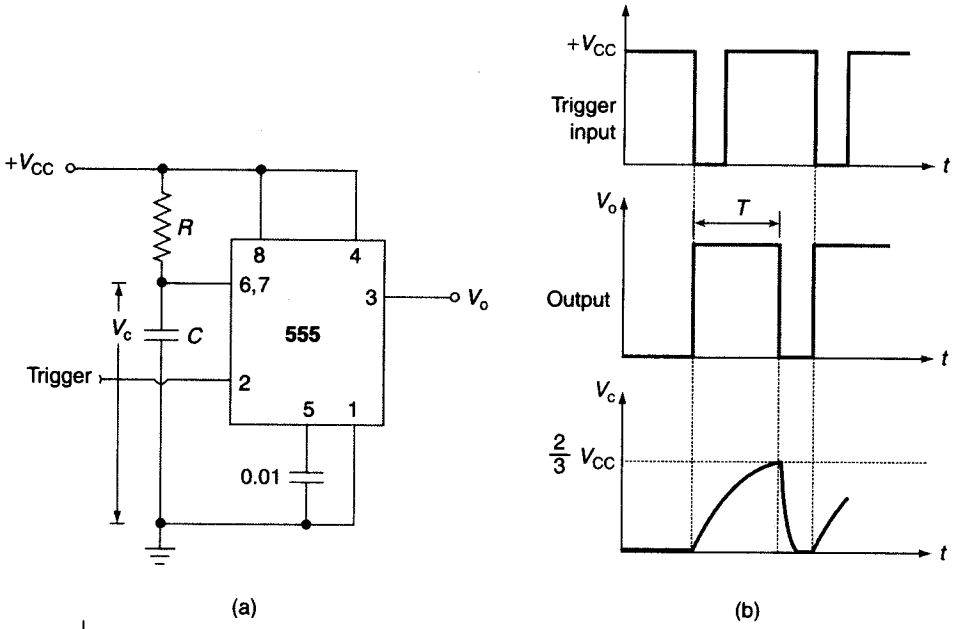



**Figure 13.52** (a) Monostable multivibrator circuit configured around timer IC 555; (b) relevant waveforms for the circuit of (a).

The pulse width of the trigger input should be less than the HIGH-time of the monoshot output. Also, it is often desirable to trigger a monostable multivibrator either on the trailing (HIGH-to-LOW) or leading edges (LOW-to-HIGH) of the trigger waveform. In order to achieve that, we will need an external circuit between the trigger waveform input and Terminal-2 of timer IC 555. The external circuit ensures that Terminal-2 of the IC gets the required trigger pulse corresponding to the desired edge of the trigger waveform. Figure 13.53(a) shows the monoshot configuration that can be triggered on the trailing edges of the trigger waveform.

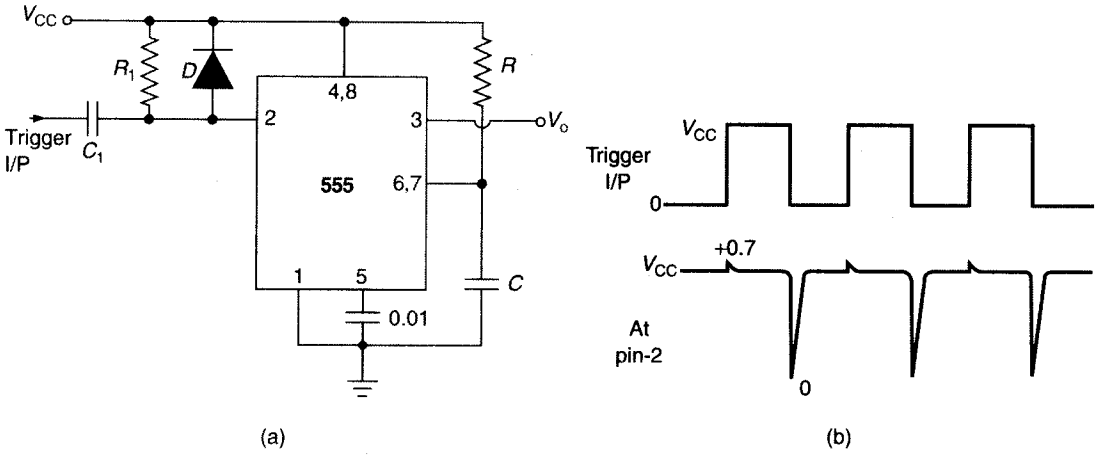



**Figure 13.53** (a) Timer IC 555 monoshot configuration triggered on the trailing edges; (b) relevant waveforms.

$R_1$–$C_1$ constitutes a differentiator circuit. One of the terminals of resistor $R_1$ is tied to $+V_{CC}$ with the result that the amplitudes of differentiated pulses are $+V_{CC}$ to $+2V_{CC}$ and $+V_{CC}$ to ground, corresponding to leading and trailing edges of the trigger waveform, respectively. Diode $D$ clamps the positive-going differentiated pulses to about +0.7 V. The net result is that the trigger terminal of timer IC 555 gets the required trigger pulses corresponding to HIGH-to-LOW edges of the trigger waveform. Figure 13.53(b) shows relevant waveforms.

Figure 13.54(a) shows the monoshot configuration that can be triggered on the leading edges of the trigger waveform. $R_1$–$C_1$ combination constitutes the differentiator producing positive and negative pulses corresponding to LOW-to-HIGH and HIGH-to-LOW transitions of the trigger waveform. Negative pulses are clamped by the diode and the positive pulses are applied to the base of a transistor switch. Collector terminal of the transistor feeds the required trigger pulses to Terminal-2 of the IC. Figure 13.54(b) shows relevant waveforms.

For the circuits shown in Figures 13.53 and 13.54 to function properly, values of $R_1$ and $C_1$ for the differentiator should be chosen carefully. First, differentiator time constant should be much smaller than the HIGH-time of the trigger waveform for proper differentiation. Second, differentiated pulse width should be less than the expected HIGH-time of the monoshot output.

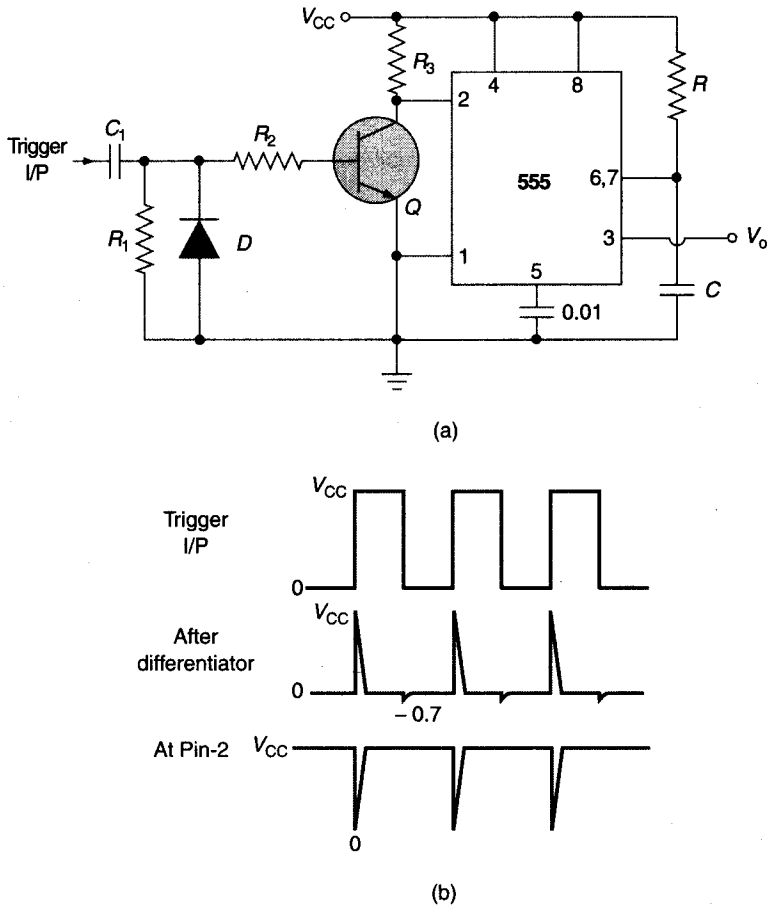



**Figure 13.54** (a) Timer IC 555 monoshot configuration triggered on the leading edges; (b) relevant waveforms.

**EXAMPLE 13.15** *Pulsed waveform of Figure 13.55(b) is applied to the RESET terminal of astable multivibrator circuit of Figure 13.55(a). Draw the output waveform.*

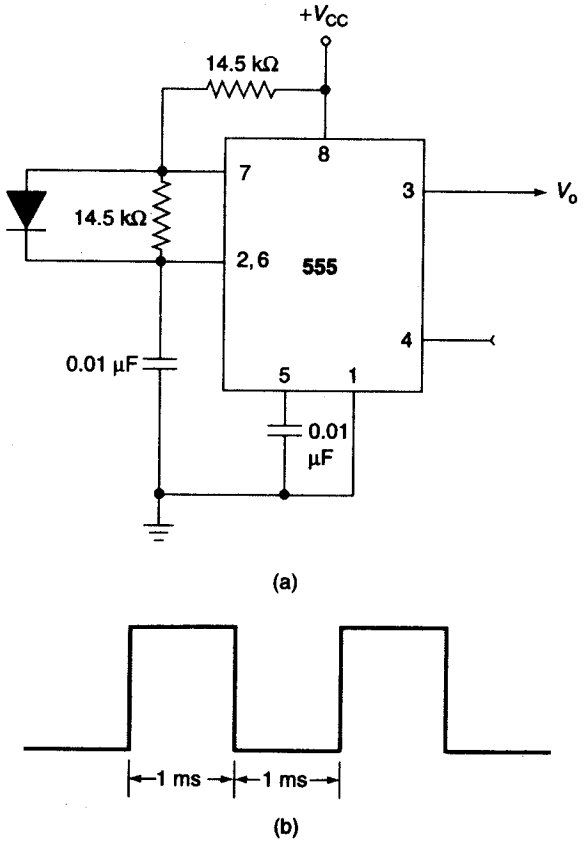



**Figure 13.55** | Example 13.15

**Solution**

1. The circuit shown in Figure 13.55(a) is an astable multivibrator with a 500 Hz symmetrical waveform applied to its RESET terminal. The RESET terminal is alternately HIGH and LOW for 1.0 ms.
2. When the RESET input is LOW, the output is forced to the LOW-state. When the RESET input is HIGH, astable waveform appears at the output.
3. HIGH and LOW time periods of the astable multivibrator are determined as follows:

   HIGH-time = $0.69 \times 14.5 \times 10^3 \times 0.01 \times 10^{-6} = 100\ \mu s$

   LOW-time = $0.69 \times 14.5 \times 10^3 \times 0.01 \times 10^{-6} = 100\ \mu s$
4. Astable output is thus a 5 kHz symmetrical waveform. Every time RESET terminal goes HIGH for 1.0 ms, five cycles of 5 kHz waveform appear at the output. Figure 13.56 shows the output waveform appearing at Terminal-3 of timer IC.

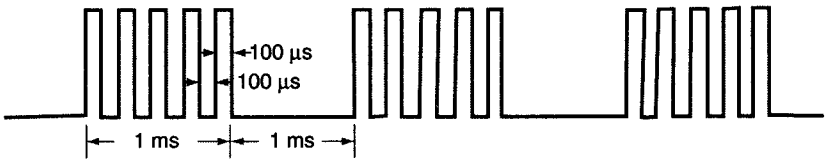



**Figure 13.56** | Solution of Example 13.15.

**EXAMPLE 13.16**

*Refer to monostable multivibrator circuit of Figure 13.57. Trigger terminal (pin-2 of the IC) is driven by a symmetrical pulsed waveform of 10 kHz. Determine the frequency and duty cycle of the output waveform.*

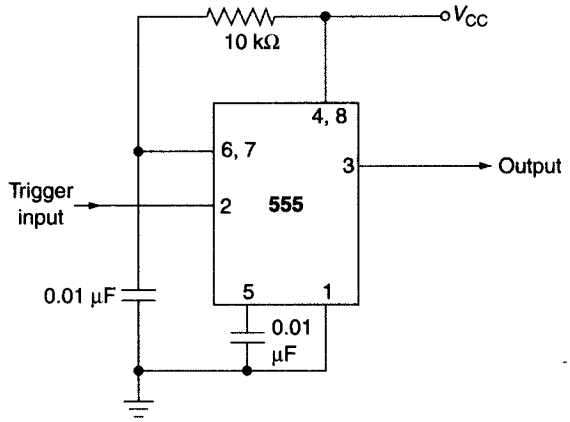



**Figure 13.57** | Example 13.16.

**SOLUTION**

1. Frequency of trigger waveform = 10 kHz.
2. Time period between two successive leading or trailing edges = 100 µs.
3. Expected pulse width of monoshot output = $1.1RC = 1.1 \times 10^4 \times 10^{-8} =$ 110 µs.
4. Trigger waveform is a symmetrical one; it has HIGH and LOW time periods of 50 µs each.
5. Since the LOW-state time period of the trigger waveform is less than the expected output pulse width, it can successfully trigger the monoshot on its trailing edges.
6. Since the time period between two successive trailing edges is 100 µs and the expected output pulse width is 110 µs; therefore, only alternate trailing edges of trigger waveform will trigger the monoshot.
7. Frequency of output waveform = $10 \times 10^3/2 = 5$ kHz.
8. Time period of output waveform = $1/(5 \times 10^3) = 200$ µs.
9. Therefore, duty cycle of output waveform = 110/200 = 0.55.

## KEY TERMS

Astable multivibrator
Bistable multivibrator
Clamping circuit
Clipping circuit
Monostable multivibrator
Multivibrator
RC high-pass circuit
RC low-pass circuit
Retriggerable monostable multivibrator
Schmitt trigger
Timer IC 555

## OBJECTIVE-TYPE EXERCISES

### *Multiple-Choice Questions*

1. A low-pass circuit can also possibly be
   **a.** an integrator circuit.
   **b.** a differentiator circuit.
   **c.** either a differentiator or an integrator circuit.
   **d.** none of these.
2. A high-pass circuit can also possibly be
   **a.** an integrator circuit.
   **b.** a differentiator circuit.
   **c.** either a differentiator or an integrator circuit.
   **d.** none of these.
3. A low-pass circuit with a relatively higher upper 3 dB cut-off frequency will
   **a.** have relatively more sluggish step response.
   **b.** have relatively steeper step response.
   **c.** behave more like an integrator.
   **d.** none of these.
4. A low-pass circuit is fed with a periodic waveform of time period $T$. For this circuit to function like an integrator, the necessary condition to be satisfied is
   **a.** $RC = T$.
   **b.** $RC << T$.
   **c.** $RC >> T$.
   **d.** none of these.
5. In the basic clamper circuit, positive or negative, a resistance $R$ is always connected across the diode. If the forward-biased and reverse-biased resistances of the diode were 10 Ω and 10 MΩ, respectively, the most optimum value of $R$ would then be
   **a.** 10 Ω
   **b.** 10 MΩ
   **c.** 100 kΩ
   **d.** 10 kΩ
6. An RC integrator circuit with an upper 3 dB cut-off frequency of 3.5 kHz will respond to a step input with a rise time of
   **a.** 100 μs
   **b.** 10 μs
   **c.** 100 ms
   **d.** indeterminate from given data.
7. An RC differentiator circuit with a lower 3 dB cut-off frequency of 3.5 kHz will respond to a step input with a rise time of
   **a.** 100 μs
   **b.** 10 μs
   **c.** 100 ms
   **d.** practically nil value.
8. In the case of an timer IC-based monostable multivibrator circuit, the requirement for the trigger pulse appearing at trigger terminal of IC timer is the following:
   **a.** Trigger pulse width should be equal to the intended output pulse width.
   **b.** Trigger pulse width should be less than the intended output pulse width.
   **c.** Trigger pulse width should be greater than the intended output pulse width.
   **d.** None of these.
9. A retriggerable monostable multivibrator is designed for an output pulse width of 400 μs. If it were fed with 11 trigger pulses with successive trigger pulses separated by 10 μs, the output pulse width would be
   **a.** 100 μs
   **b.** 400 μs
   **c.** 500 μs
   **d.** 200 μs

10. A Schmitt trigger circuit is a type of
    a. bistable multivibrator circuit.
    b. monostable multivibrator circuit.
    c. astable multivibrator circuit.
    d. none of these.

## REVIEW QUESTIONS

1. Draw the basic single-section RC low-pass circuit and briefly explain how does this circuit respond to a step input and a pulse input of given time duration? Under what conditions does this circuit behave as an integrator?
2. Prove that:
    a. Low-pass RC circuit responds to a step input with a rise time of $0.35/f_U$, where $f_U$ is the upper 3 dB cut-off frequency.
    b. Upper 3 dB cut-off frequency in the case of a single-section low-pass RC circuit is given by $1/2\pi RC$.
3. Draw the basic single-section RC high-pass circuit and briefly explain how does this circuit respond to a step input and a pulse input of given time duration? Under what conditions does this circuit behave as a differentiator?
4. With the help of relevant circuit diagrams, briefly describe the operation of clipping circuits that can be used to:
    a. Clip portion of positive half cycles of a sinusoidal input with amplitude greater than a certain specified DC voltage $V_{BB}$, assuming that the peak amplitude of sinusoidal input is greater than $V_{BB}$.
    b. Clip portion of negative half cycles of a sinusoidal input with amplitude more negative than a certain specified DC voltage $-V_{BB}$, assuming that the peak amplitude of sinusoidal input is greater than $V_{BB}$.
5. With the help of circuit diagram, briefly describe the operation of a positive clamper circuit. What is role of resistor ($R$) in the clamping circuit? How does one choose an optimum value of the resistance?
6. Distinguish between bistable, monostable and astable multivibrators. How does a bistable multivibrator differ from a Schmitt trigger circuit from the viewpoint of both the circuit schematic and function?
7. How does a retriggerable monostable multivibrator differ from a conventional monostable multivibrator? What determines the output pulse width in the case of a retriggerable monostable multivibrator?
8. With the help of circuit diagram, briefly describe the operation of timer IC-based astable multivibrator in which output HIGH- and LOW-state time periods can be set independently.
9. With the help of circuit diagram, briefly describe the operation of timer IC-based monostable multivibrator that can be triggered on
    a. HIGH-to-LOW transitions of input pulse train.
    b. LOW-to-HIGH transitions of input pulse train.
10. Briefly describe reasons for the following:
    a. Why are diode-based clipping circuits also called non-linear wave shaping circuits?
    b. Why should the trigger pulse appearing at trigger terminal of the IC timer 555 in a monostable multivibrator configuration be less than the expected output pulse width for intended operation?
    c. Why does a low-pass RC circuit behave as an integrator when the RC time constant is much larger than the time period of the input waveform?

## PROBLEMS

1. A simple low-pass RC network is fed with a 10 V step. If $R$ = 10 kΩ and $C$ = 0.1 μF, what will be the time period in which the output will change from 1.0 V to 9.0 V?
2. The RC network of the type of Problem 1 with different values of $R$ and $C$ gives a rise time of 100 μs to a certain step input. Determine the 3 dB cut-off frequency of the network.
3. Determine the most optimum value of $R$ in the clamper circuit of Figure 13.58 given that forward-biased and reverse-biased resistances of the diode are 10 Ω and 10 MΩ, respectively.

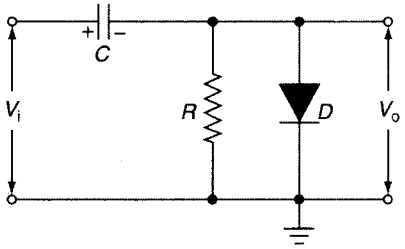



**Figure 13.58** | Problem 3.

4. Refer to the astable multivibrator circuit of Figure 13.59. It is given that $V_{CC}$ = + 5 V, $R_1 = 2R_2$. If the LOW-state time period of the output waveform were 1 ms, draw the output waveform.

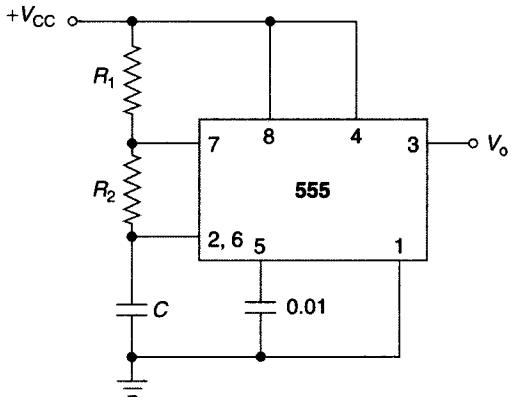



**Figure 13.59** | Problem 4.

5. The monostable configuration of Figure 13.60 was designed by some one to generate a pulse (pulse width of course depending upon the values of $R$ and $C$) whenever it was triggered by the available trigger pulse as shown. The circuit did not seem to work. What would be wrong with the circuit?

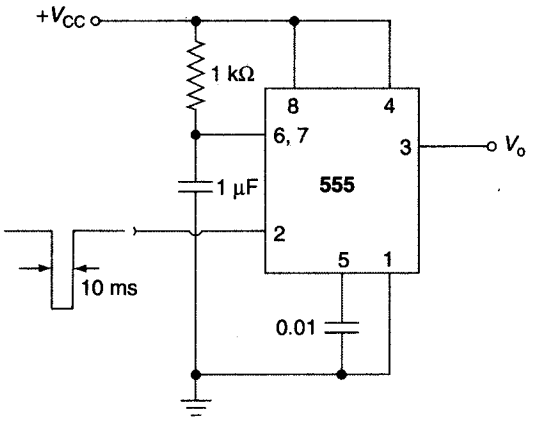



**Figure 13.60** | Problem 5.

# ANSWERS

## Multiple-Choice Questions

| | | | | |
|---|---|---|---|---|
| **1.** (a) | **3.** (b) | **5.** (d) | **7.** (d) | **9.** (c) |
| **2.** (b) | **4.** (c) | **6.** (a) | **8.** (b) | **10.** (a) |

## Problems

**1.** 2.2 ms
**2.** 3.5 kHz
**3.** 10 kΩ
**4.** Figure 13.61

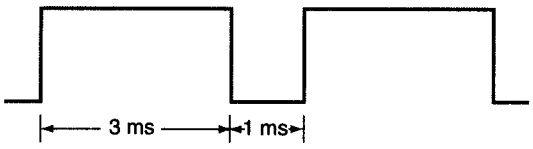



**Figure 13.61** Solution to Problem 4.

**5.** Trigger pulse width appearing at pin-2 of the IC is greater than the expected output pulse width. It should be less than the expected output pulse width.